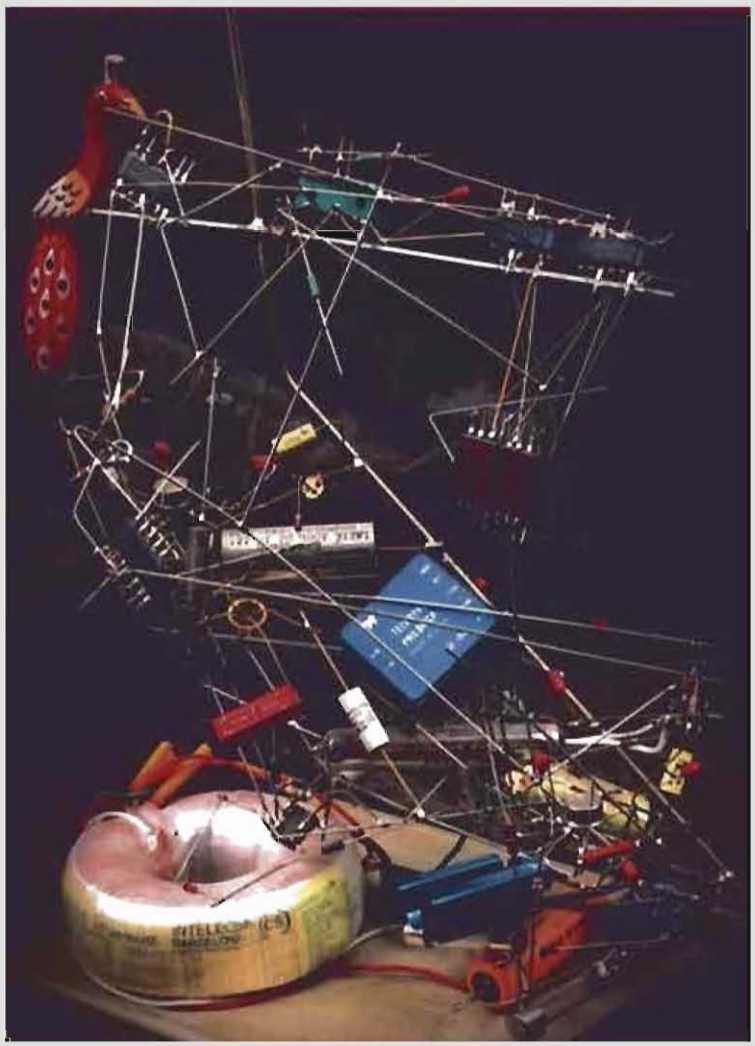
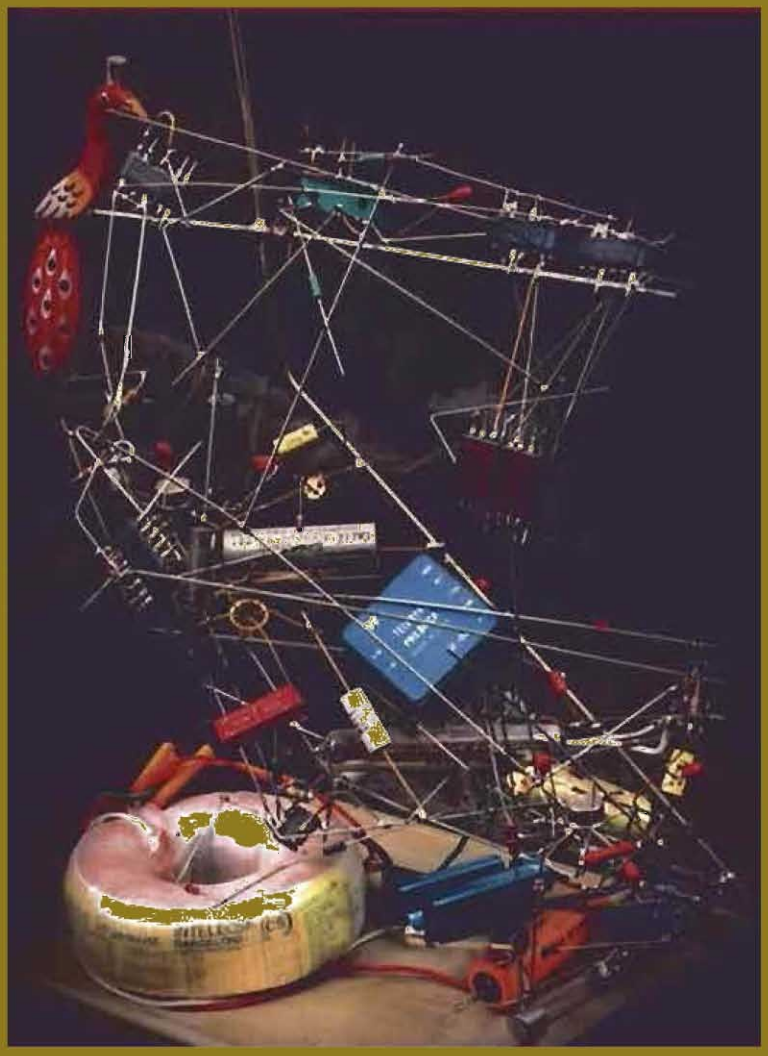
A Tribute to Jim Williams

Electronic Design (1974-2008)



A Tribute to Jim Williams

Electronic Design (1974-2008)



Split a temperature degree to 10 μ°C. Use a linear-dc-feedback circuit, watch the grounding and thermal, magnetic and electric shielding, and put in only quality components.

Suppose you have to set a temperature to high resolution and hold it within 10 μ°C. Can you find a commercial unit that will do it? Probably not. To split the degree this fine, you need a custom, high-gain, linear circuit to control dc current.

Many of the available temperature-controlled instrument ovens are of the bang-bang variety. The rest, though called proportional controllers, may not even hold to a degree centigrade. Such controllers often use SCR drives for the heating elements, and the 60-Hz pulsing of the power to the heater could easily overshoot a 10-μ°C requirement.

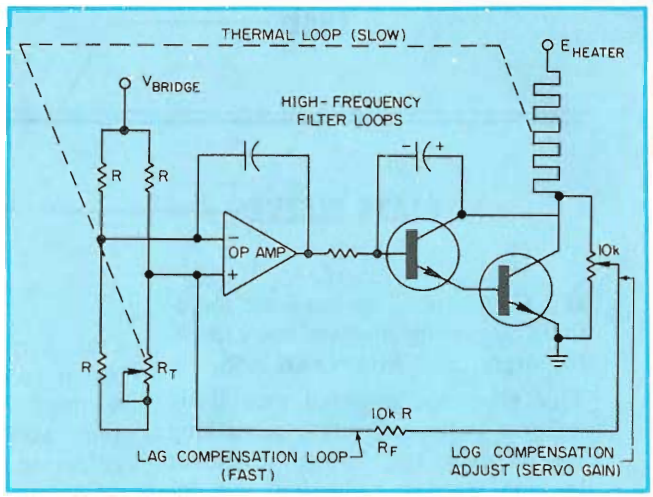
Yet many applications exist for a temperature controller with microdegree capability.[1] Examples include studies in the following fields:

- Laser microinterferometry.
- Zener-reference temperature compensation.
- Crystal growing.
- Transition points of positive-temperature-coefficient ceramics.
- Biological calorimetry in picowatts. A human cell operates at about 1 nW. Single-cell calorimetry is a possibility.

Replace energy at the rate lost

To control temperatures above ambient, you must replace the energy at the same rate that the system loses it. If a perfect heat insulator were available, the energy could be raised to the desired level and the current shut off. The job would be done. But any oven left without power eventually assumes the temperature of its surroundings.

The simplified schematic of a dc feedback loop, as used in the MIT Nutrition and Food Science oven, meets the requirements of a microdegree controller (Fig. 1). Assume that the lag-compensation potentiometer is at its lowest setting and that the system has just been turned on. With the oven cold, the negative-temperature-coefficient thermistor, R_T, has a relatively high resistance—say, 3R.



1. **The temperature controller's simplified feedback system** shows the thermal and electric feedback paths.

The unbalanced bridge saturates the op amp into its positive region. The 10-kR resistor, R_F, is too large to have any effect now. The Darlington power-output pair immediately saturates, and full dc power is delivered to the heater.

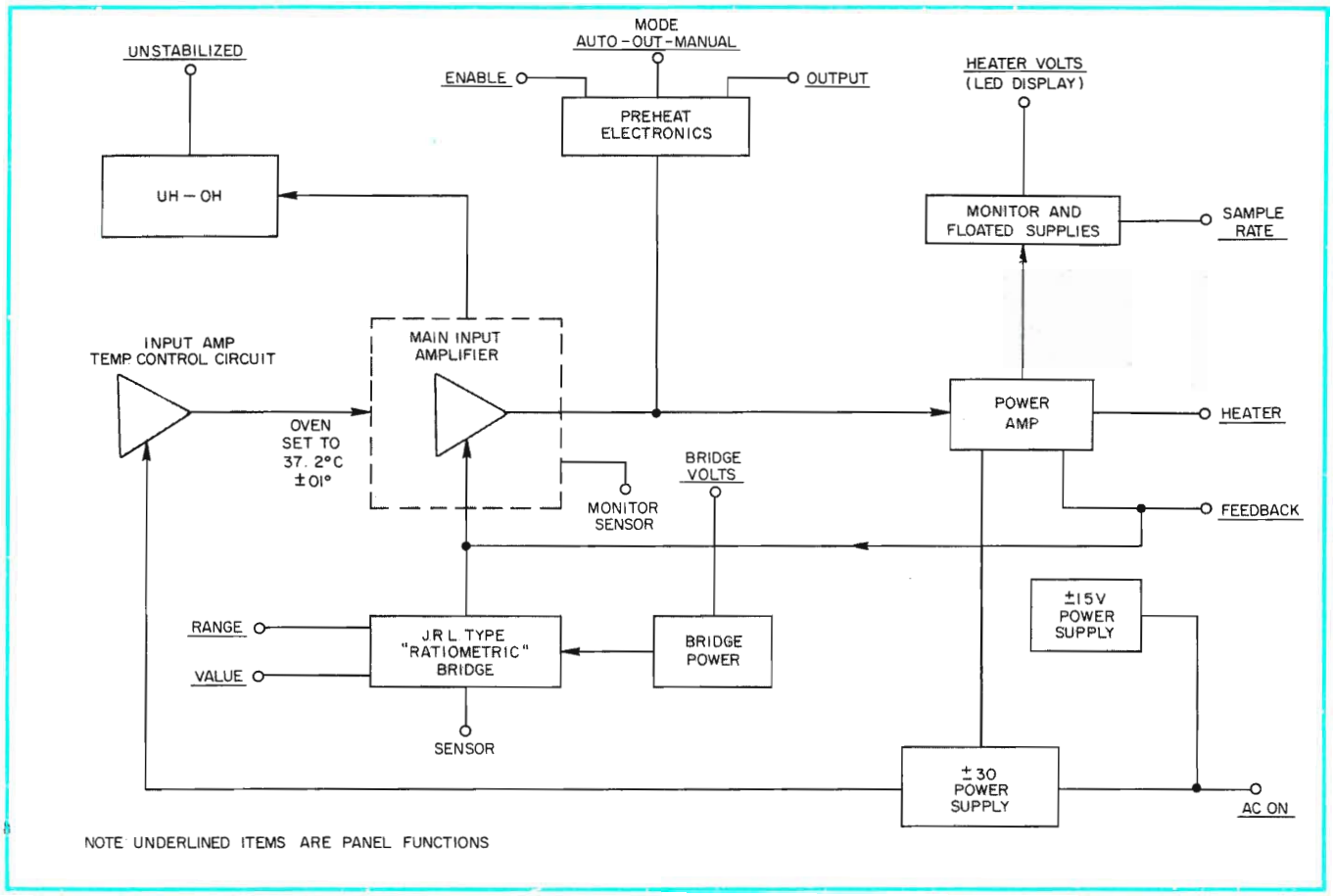
As the heater warms, the bridge balance shifts, and its output polarity soon reverses to drive the op amp into negative saturation. The Darlington pair cuts off, and the heater goes off. The process repeats after the oven cools. The circuit is now operating as a high-gain, bang-bang controller—which, of course, is not the objective.

The high gain of the op amp, the gain of the Darlington pair and the thermal lag between heater and sensor create an ideal condition for the oscillations. To stop this, either the gain must be reduced or the thermal time lag brought to zero. The latter is not possible, but the former is. The lag-compensation control can reduce the dc gain of the system.

Note that, because the Darlington circuit inverts, the lag-compensator adjustment provides negative feedback to the noninverting input of the op amp.

The capacitors shown in the op-amp's feedback

Dr. James Williams, Dept. of Nutrition and Food Science, MIT, Cambridge, Mass. 02139.



2. **Auxiliary circuits,** such as a separate temperature control for the main input amplifier and a preheater, are essential for stability and convenience. All power is regulated and the bridge supply is variable.

path limit the high-frequency response of the circuit and help provide rejection of 60 Hz and any other unwanted high-frequency components.

After the gain is reduced so the system ceases to bang-bang between saturation points of the op amp, the objective is to retain the maximum possible gain. However the system must avoid any tendency to self-oscillate sinusoidally. Typically such oscillations occur in the 1-Hz range. Any tendency toward periodicity in the heater voltage indicates that the system loop gain is still too high. The feedback must be adjusted until the heater voltage shows only small, random, variations (see box).

Input circuit is critical

The principles of the feedback circuits in this microdegree temperature controller are, of course, not new (Fig. 2). Success depends upon meticulous wiring, assembly and component selection.

The controller can't be a clip-lead-and-breadboard job. Don't use a shield as a current carrier, don't ground both ends of a shield, and don't use BNC connectors. Banana plugs are better. Better yet, use securely soldered joints. Shielded leads to sensors and instruments should expose a minimum of unshielded wire.

Protect all input components and circuits from any widely varying ambient changes, and observe all the traditional grounding rules. A ground loop of only 2 in. of wire can cause a 10% change in heater current. Use only the most stable and reliable components, especially in the input circuit. Substitutes for the key components are not advised.

Coddle the input circuits

The input circuit is critical to the long-term stability of the temperature controller. Thus the input-sensor bridge circuit and the input amplifier must receive special treatment.

The sensor bridge is different from the ordinary Wheatstone bridge. The sensor bridge arrangement, developed by Julie Research Laboratories in New York City, uses a fixed-impedance, Kelvin-Varley divider[2] as one variable element in the bridge over many decades of resistance, and each decade has a linear resistance scale. The input bridge can accommodate a wide range of thermistor resistances and corresponding selected temperatures. This bridge arrangement, and the

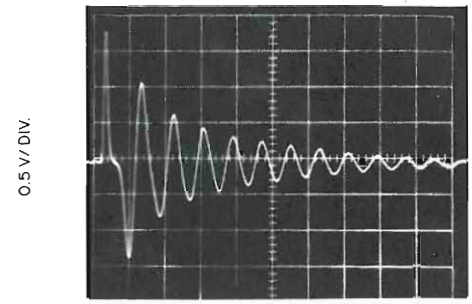
How to tune the temperature controller

The microdegree temperature controller requires exacting adjustment to attain its ultimate stability. Start with the lag-compensator-adjustment potentiometer in zero position. Then gradually increase the pot's output. This increases the loop's feedback and reduces the overall system gain, until the heater-voltage oscillations appear sinusoidal (see oscillograph traces). The system is now operating in its linear range and behaves more like a linear servo. Continue to increase the potentiometer setting slowly until the oscillations tend to dampen out.

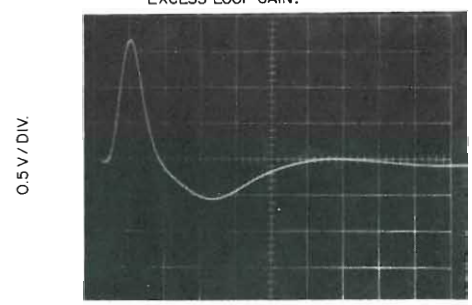
Now give the system a step function: Change the temperature set point by perhaps 500 microdegrees. This can be done if you vary one of the bridge resistors slightly. If there is too much gain, the loop will ring (a). Reduce the gain further until a minimum amount of ringing is produced (b).

The thermal loop is at its best setting when random variations are obtained with the controller at equilibrium (c). Note the absence of any dominant periodic components, which would indicate that the loop was trying to oscillate.

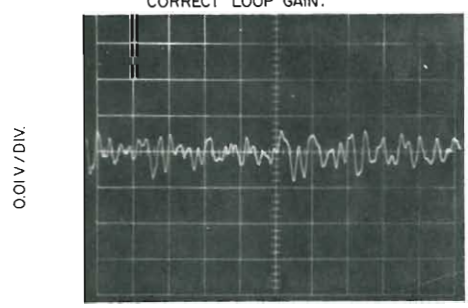
An interesting phenomenon occurs after the oven walls first reach their equilibrium control point. Although the temperature across the walls is constant, the current through the heater drops at a perceptible rate. This seeming paradox occurs because less and less energy is taken from the walls as the oven's contents approach saturation, and the controller backs off the heater power to maintain control. When saturation finally occurs, the voltage level across the heater stabilizes about a point that is dependent ultimately on room ambient and the oven's insulation characteristics. The controller's corrections are random adjustments about the equilibrium heat level as ambient changes and other fluctuations occur. Once saturation is attained, it's wise to check the lag-compensation gain setting, again, after several hours or days.



(a) – RESPONSE TO A 500 μC STEP WITH EXCESS LOOP GAIN.



(b) – RESPONSE TO A 500 μC STEP WITH CORRECT LOOP GAIN.



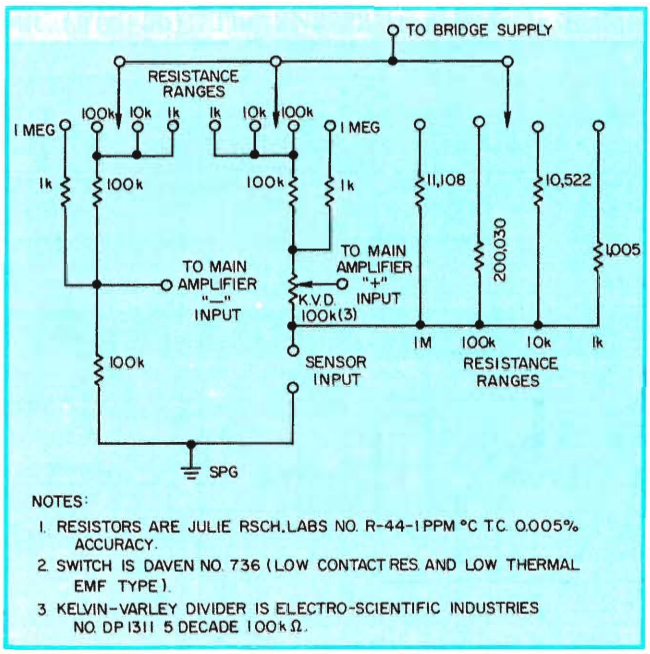
(c) – RANDOM HEATER ADJUSTMENTS TO MAINTAIN OVEN TEMPERATURE, WHEN LOOP GAIN IS CORRECT.

NOTE: ALL READINGS ARE AC COUPLED TO OSCILLOSCOPE. DC LEVEL APPROXIMATELY 5V.

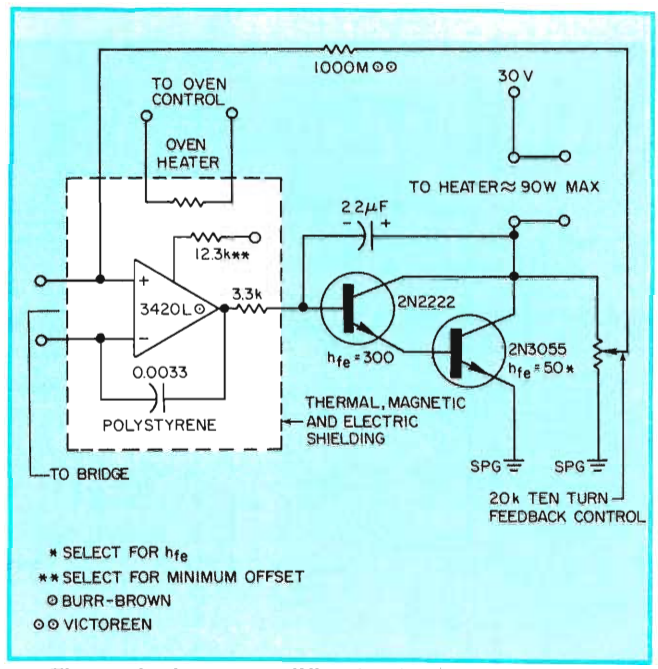
very stable precision resistors used in the fixed arms, make the system easy to use. Of course, all the other components in the input bridge must also be of the highest quality to ensure long-term stability. The region of 10 μ°C stability tolerates no compromise.

Experience with the system shows that sensors that operate in the 1-kΩ range should not be used, if you wish to attain the highest stability. The higher resistance ranges are less subject to See-back effects and connector and switch contact-resistance variations. The MIT oven uses a Yellow Springs Instrument Co. Sensor, No. 44014.

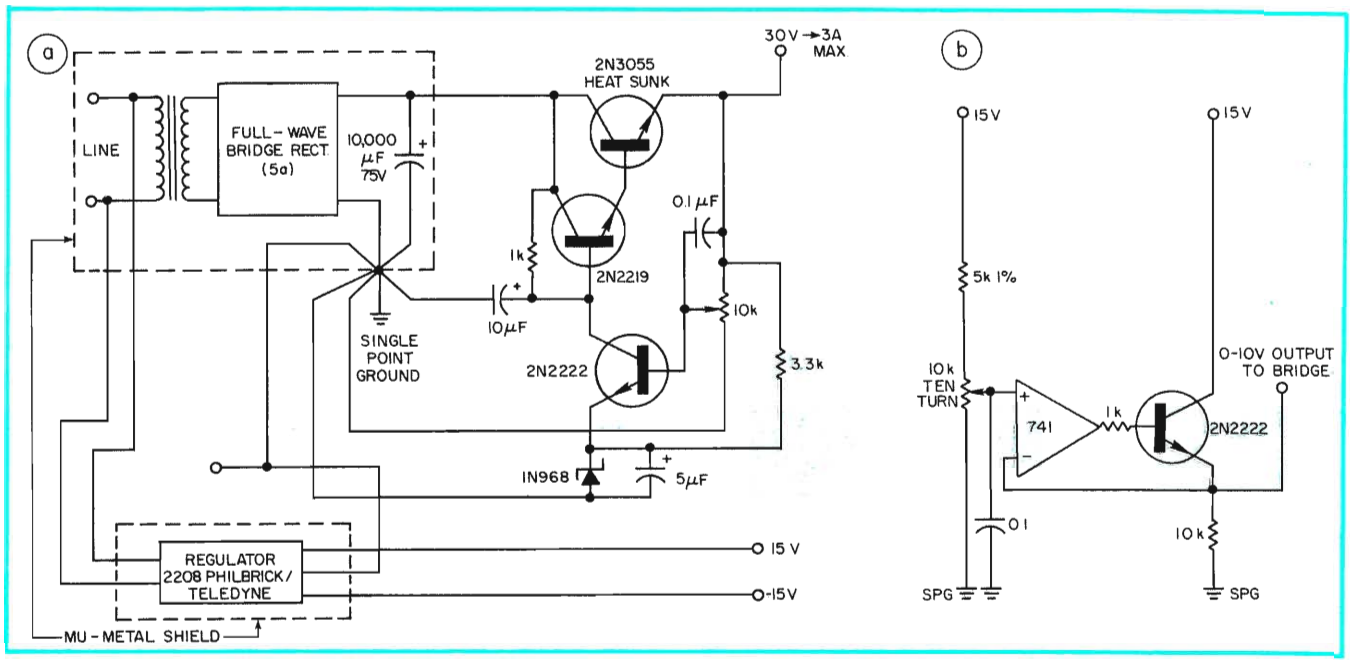
The system's input amplifier is particularly coddled (Fig. 4). The amplifier is shielded from the ambient electrostatically, magnetically and thermally. An instrument oven that uses a detuned version of the main temperature-control circuit keeps out any thermal transients of the ambient and rate coupling from the system's



3. **The sensor bridge** uses a Kelvin-Varley divider in one of its arms to provide a linear resistance scale and to enable the bridge to match a wide range of temperatures and sensors.



4. **The main input amplifier** is thermally, magnetically and electrically shielded. A separate heat regulator circuit (Fig. 6) provides the thermal isolation and very special attention is paid to grounding.



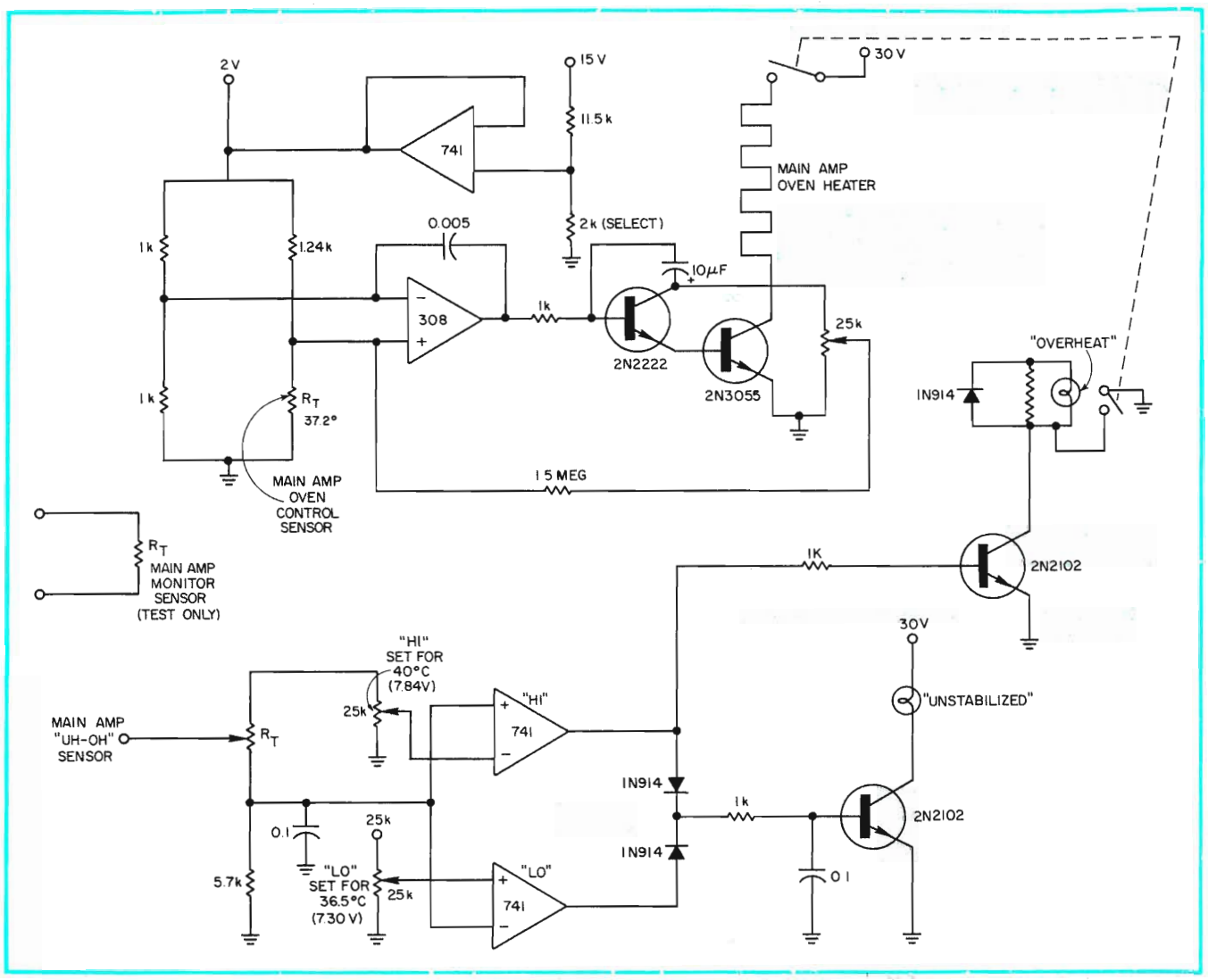
5. **Power supplies** for the heater element and amplifiers (a) and bridge (b) are regulated. The ±15-V supply for the amplifiers is enclosed in a Mu-metal magnetic shield.

heater. The oven is set to maintain 37.2 ±0.01 C.

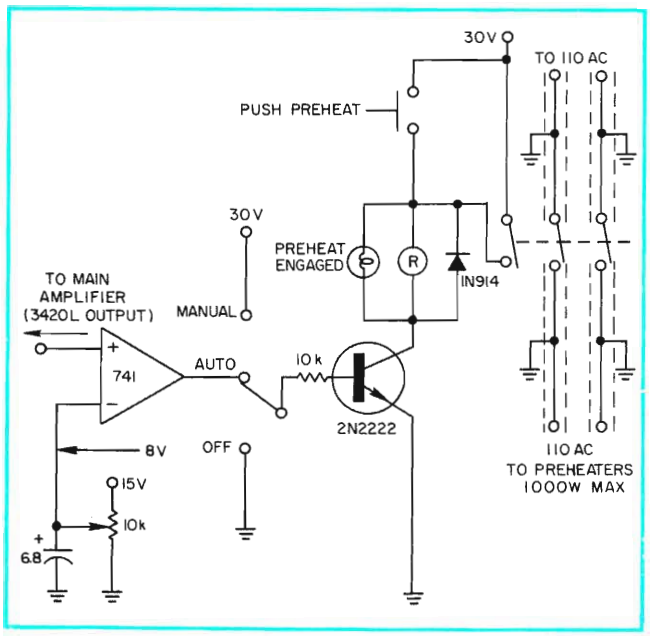
A Burr-Brown 3420L amplifier, with 1-pA bias current and a 90-dB common-mode rejection ratio, allows the use of high-impedance input sensors. And the amplifier's 1-μV/°C offset drift, combined with the ±0.01-C controlled oven, leaves only the sensor noise as the dominant error factor.

Also, every connection to the amplifier is shielded. Finally the 3.3-kΩ resistor at the amplifier's output helps prevent excessive loading and heating of its output transistors. This resistor also maintains the amplifier's gain and reduces the possibility of a thermal "tail" within the module.

Fig. 4 also shows the power amplifier, which consists of a 2N2222 transistor that drives a 2N3055 in a Darlington configuration. The output amplifier can control a 90-W-maximum heater with a 30-V power supply. A 10-turn potenti-



6. **The input amplifier** is protected by a special temperature-controlled oven and held at 37.2 ±0.01°C.



7. **A preheater circuit** for high-heat-capacity systems greatly speeds the temperature controller's start-up.

ometer serves as the lag-compensation adjustment to control the feedback and to set the system's over-all gain.

Regulated power supplies needed

The power supplies required are ±15 V at 100 mA for the system's various op amps and other circuits, +30 V at 3-A max for heater power (Fig. 5a) and a 0 to 10-V source for the bridge (Fig. 5b). The ±15 V is derived from a Philbrick 2208 module, and the +30-V supply provides 1% regulated power with a classic series-pass arrangement. The 2N3055 series transistor is mounted on the unit's rear panel to keep out the transistor's heat. Both the ±15 and +30-V supplies are Mu-metal shielded to keep the transformer field from interfacing with the sensitive amplifiers.

The bridge supply is simply a unity-gain, op-amp follower that is boosted with a 2N2222 out-

put (Fig. 5b). The 2N2222 transistor is inside the feedback loop to take care of the transistor's drifts. The 741 amplifier input is derived from a 10-turn potentiometer that has 10 V across it. Thus the output voltage to the bridge can be read directly on a turns-counting dial, since the 741 loading on the pot is negligible. It is best to keep the bridge voltage low to avoid drift and noise problems. The sensor manufacturer's specs should be consulted for the best setting.

The combination of very small input currents and large heater currents can provide serious grounding problems unless a single-point-return technique is employed. A 1/4 × 4 × 1.5-in. tinned-copper plate serves as the ground "point." All returns terminate at this plate, and no ground busses are used in the unit.

Auxiliary circuits are important, too

The rest of the circuits are auxiliary to the main input amplifier, power amplifier and power supplies, but they make important contributions to the system's stability and ease of use.

The input-amplifier oven circuit operates similarly to the main system (Fig. 6). The whole circuit is inside a 5 × 3-in. aluminum cylinder, with a 0.5-in. wall enclosed in a small Thermos bottle. An aptly named "UH-OH" (Underheat-Overheat) circuit provides a go-no-go indication of the oven's status. A double-limit comparator, which uses two 741 amplifiers, monitors the voltage established by the UH-OH thermistor sensor and a 5.7-kΩ resistor. If the voltage goes out of the bounds set by the low and high potentiometers, an "Unstabilized" indicator will light. Further, if the high comparator is tripped by the oven overheating, a relay latches and removes the heater power from the control circuit.

The Unstabilized indicator lights when the instrument is turned on. When the oven comes up to temperature, the bulb goes out. Thereafter if the bulb comes on again, a circuitry malfunction is indicated.

A second bulb connected across the relay contacts, when lighted, indicates that the failure was due to oven runaway. This elaborate protection scheme was considered necessary because the input amplifier is a key item in the system's performance, and it can be readily damaged by a runaway oven.

A preheater speeds the work

A preheater circuit can be provided to raise the temperature of a high-heat-capacity system rapidly (Fig. 7). Such a circuit has 1000-W auxiliary heaters. Once the operating temperature is reached, the preheater turns off automatically.

A 741 amplifier in the preheater acts as a comparator and swings into positive saturation when the temperature controller is turned on. When the preheater's switch is in the auto position, a 2N2222 transistor actuates a relay when the Push-Preheat button is depressed. The relay latches and delivers power. When the oven gets to the selected control point, the 3420L main input amplifier swings negative, the 2N2222 cuts off and de-energizes the relay. The main temperature-controller circuit then automatically takes over.

From the block diagram of Fig. 2, we see that the heater voltage of the controller is monitored by a digital voltmeter. Though the specific unit used in the MIT oven is homemade, almost any good 3-digit voltmeter will do. The heater has low impedance, so the voltmeter input resistance need not be greater than about 10 kΩ. This output monitor should float above ground and be well-isolated from the rest of the controller. ■■

Some hints on oven design

Thick oven walls help to keep the temperature stable. Cylindrical shapes are good, if you wind the heaters more densely near the ends, but spheres are the best choice for an oven's shape. Styrofoam and fiberglass are cheap and effective insulation, but Dewar flasks are best. Cascaded ovens (one inside another) are a must for ultra-high stabilities over a long time.

Baths are also helpful, because it is easy to get huge thermal capacity with them. Stir them to enhance the bath's isothermal integrating characteristic. But watch out for dead spots and layering effects. The goal is an evenly distributed heater, such as a concentric spiral.

To obtain better than 100-μ°C stabilities, you must pressure-seal dry ovens. Since $PV = nRT$, atmospheric-pressure changes produce temperature shifts.

It's common practice to specify a temperature controller in terms of temperature gain. This is defined as the ratio of ambient-temperature change to the change in the controlled environment. Hence a 1°C ambient shift will result eventually in a 10-μ°C oven shift for a temperature-gain specification of 100,000. But this spec, alone, has limited usefulness because the effects of an ambient temperature shift may take hours to stabilize.

References:

1. Williams, J., "Temperature Controlling to Micro-Degrees," MIT Educational Research Center, Oct., 1971.
2. Julie, Loebe, "Laboratory Manual for DC Measurements," Julie Research Laboratories, New York City.

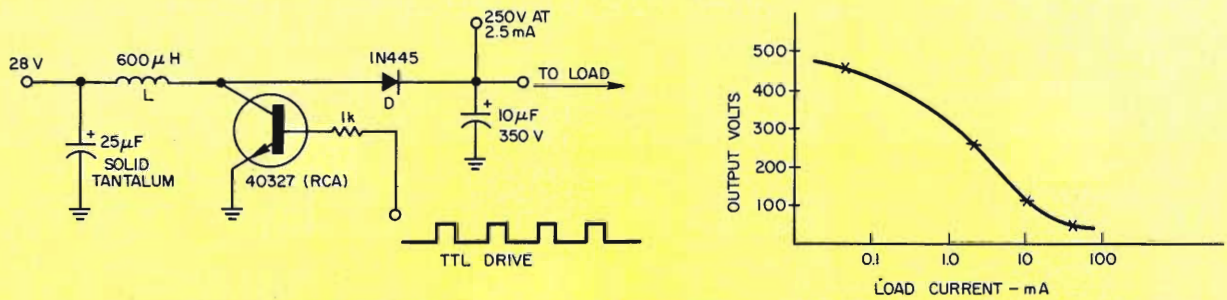
Boost transistor-level supply voltages to make a low-power, high-voltage supply

Need a small amount of high-voltage power in your transistor circuit? The simple circuit shown uses an inductor and a high-voltage switching transistor to perform a 10-to-15-times voltage multiplication with about 75% efficiency.

When transistor Q is driven into conduction by the drive input, inductor L stores energy in its magnetic field. When Q cuts off sharply, L generates a high-voltage pulse ($e = L\ di/dt$) at Q's collector. Diode D directs and isolates the pulse to a 10-μF filter capacitor and the load. The 25-μF solid-tantalum capacitor completes the discharge path for L, and bypasses the 28-V power source.

For a load of 100-kΩ, about 250 V at 2.5 mA is delivered.

James Williams, Senior Engineer, Dept. Nutrition & Food Science, Instrumentation Laboratory, Massachusetts Institute of Technology, Cambridge, Mass. 02139. CIRCLE No. 312



Small amounts of high-voltage power can be obtained with a simple inductor and high-voltage transistor.

Prevent low-level amplifier problems.

Commonplace components and assembly techniques can wreck performance. Here's how to maintain the precision you need.

Even though much progress in performance has been made in low-level circuit design for instrumentation and servo control, many problems cannot be countered without making careful tradeoffs. Aside from selecting the best amplifier, you must also consider the power supplies, grounding, shielding, bypassing and even the external components used.

Carefully designed amplifiers provide microvolt offset voltages, drifts down to 100 nV/°C and input bias currents of less than 1 pA. But even with first-rate specs like these, there are many ways you can unwittingly cripple performance. Among the things you must guard against:

- Haphazard selection of the power supply.
- Improper grounding of the circuit.
- Unprotected input signals.
- Poor choice of external resistors, capacitors and wiring techniques.

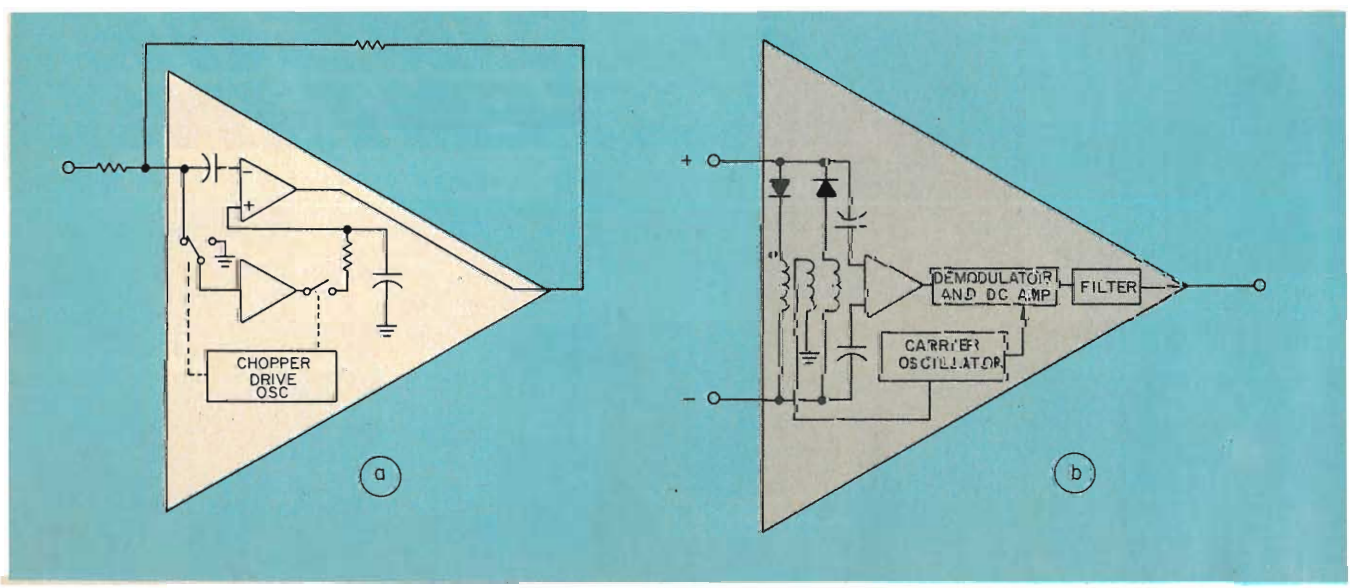
If you avoid these traps, performance can meet or surpass the manufacturer's data.

The high-stability amplifiers used in low-level circuit design are available from many manufacturers. But the variety of amplifiers presents some selection problems and calls for tradeoffs. For instance, most low-level amplifiers are limited in frequency response to a bandwidth below several kilohertz, compared with typical operational amplifiers that have responses into the megahertz region. Bandwidth vs sensitivity must be evaluated.

Two major types of low-error amplifiers are available: chopper-stabilized and varactor-bridge. Both use a carrier-modulation technique that either controls an electronic switch or excites a bridge.

A chopper-stabilized amplifier (Fig. 1a) can be built from two basic operational amplifiers. One amplifier, usually stabilized, is ac-coupled through a capacitor to the input signal to isolate the input dc offsets from an internal summing junction. The stabilized amplifier is, in turn, connected to a modulated switch that feeds the

James Williams, Senior Engineer, Instrumentation Lab, Dept of Nutrition and Food Science, Massachusetts Institute of Technology, Cambridge, MA 02139.



1. **The basic chopper-stabilized amplifier** (a) contains two separate amplifiers in a servo loop that nulls any drift. The varactor-bridge amplifier (b) has a modulated bridge input that allows extremely low bias currents.

input of the second amplifier. This switch, driven by an internal oscillator, samples the offset at the summing junction and, by use of a synchronous demodulator, drives the positive input of the stabilized amplifier, thus counteracting the amplifier's dc drift. The feedback for this servo type of action is to the chopper circuit through an external feedback resistor.

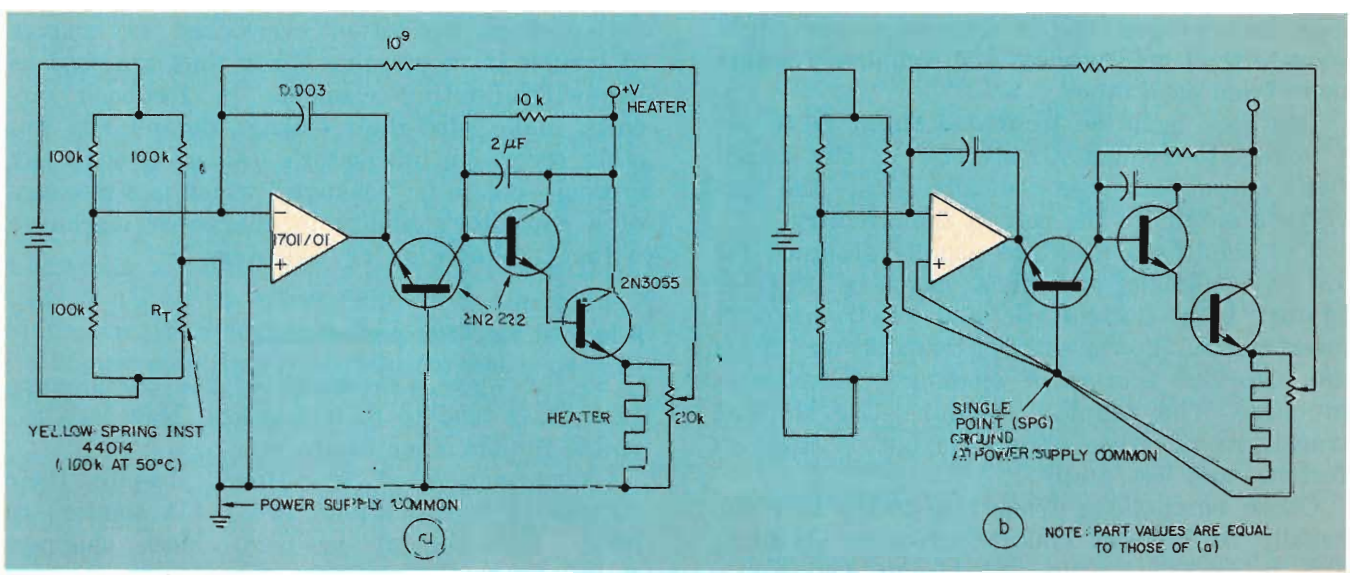
The varactor-bridge amplifier, although not chopped, uses a carrier-modulation scheme (Fig. 1b). The varactor diodes have a junction capacitance that depends upon the applied voltage. With no voltage applied, they have a high resistance in the off state. The amplifier input circuit is a floating bridge, constructed from two diodes and a modulating signal. If the inputs are precisely balanced, the diodes are equally biased and the bridge has no output. An ac input unbalance will change the diode capacitances, which in turn produces an rf output from the bridge. This signal is then amplified, synchronously demodulated and filtered to obtain a dc output signal.

Even when you have high-quality circuits, they can easily perform poorly if the components connected to them have been incorrectly selected. For instance, make sure you choose a well-regulated, low-output-impedance power supply. And watch out for these problems: Does the output of the supply overshoot when power is applied or when transients occur? Does the regulation spec include immunity to fast transients on the ac line, or do the transients feed through to the output?

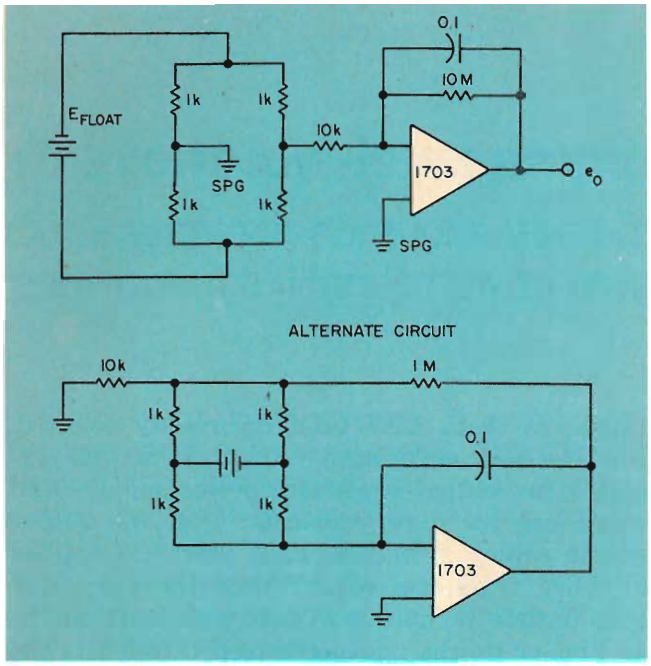
Power supplies cause problems

Series-pass, linear-regulated, power supplies are the safest choice for precision circuits; however, there are some good switching supplies. Switchers offer high efficiency and small size, but beware of the high-frequency transformer radiation—this can wreck the amplifier's input. Some switching manufacturers have solved this problem; others have not even bothered to look into it.

Some amplifier modules are equipped with internal bypass capacitors. If in doubt about the unit you have, check with the manufacturer or bypass the power-supply lines at the amplifier



2. **A precision temperature-control circuit** that has ground problems (a) uses a chopper-stabilized amplifier to provide microdegree accuracy over a predetermined range. By rearranging the ground circuit you can eliminate noise and ground loop problems (b) that can cause poor circuit operation.



3. **Single-ended chopper-stabilized amplifiers** can be connected by use of a floating-bridge circuit to perform as if they had a differential input.

with solid tantalum capacitors. Aluminum electrolytics simply do not see fast transients.

Good grounding techniques are always a must. As an example, look at the temperature-control circuit of Fig. 2. Erratic operation of this circuit can be caused by a ground bus, even when the latter is only 3 in. long and made from 12-gauge wire. Large heater currents returning through the pass transistor combined with small bridge and amplifier currents set the stage for real trouble. If heater drive comes from a separate supply, the problems become even more complex. Ground lines that have large switching currents are very noisy and usually full of fast current spiking. A nondegrading common ground must be arranged, and in some cases you might want to float both circuits and completely isolate them from each other.

One good isolation technique might be to use a voltage-to-frequency converter at the amplifier's output and then optically isolate the converter's output to the rest of the circuitry.

The amplifiers used are usually designed for low-level signals and thus must be shielded against both electrostatic and electromagnetic interference. Power-supply transformer fields are notorious sources of seemingly inexplicable problems. The simplest solution: Use shielded transformers. More careful layout is also effective—and less costly.

Other emanations from the 60-Hz line can usually be brought under control by shielding and deliberate limiting of circuit bandwidth. Battery-powered circuits, despite their "line isolation," are susceptible to 60-Hz pickup. A few picofarads of ground capacitance can seriously degrade the performace of a circuit like that in Fig. 6.

Components add unwanted headaches

Although not generally considered components, wire, solder and insulation must be considered. Certain combinations of solder, wire and binding posts can generate thermal emf's. For example, a junction of stranded wires from two different manufacturers can easily produce an emf of 200 nV/°C, or twice the input drift of an amplifier like the Teledyne Philbrick 1701/01. Amplifier sockets are fine, but a poor one can introduce contact resistance, thermal potentials or both.

With varactor amplifiers the socket choice is highly critical—10^{15}-Ω leakage from the power-supply pins to the input can provide almost 10 times the required bias current. Teflon sockets are the best choice for minimal leakage. On the circuit board, critical circuit paths should be guarded.

Precision metal-film resistors are good, but some are better than others. Certain types use "end cap" terminations and can produce pronounced thermocouple effects that swamp out a good amplifier's drift spec. High-grade wire-wound resistors offer the ultimate in low-noise performance, but they are also expensive and relatively large; save them for applications where absolute accuracy, high stability or very low temperature coefficients are musts. For example, the circuit in Fig. 2 can maintain very good stability without wire-wound resistors if you select metal-film resistors that have a 5-ppm tracking temperature coefficient.

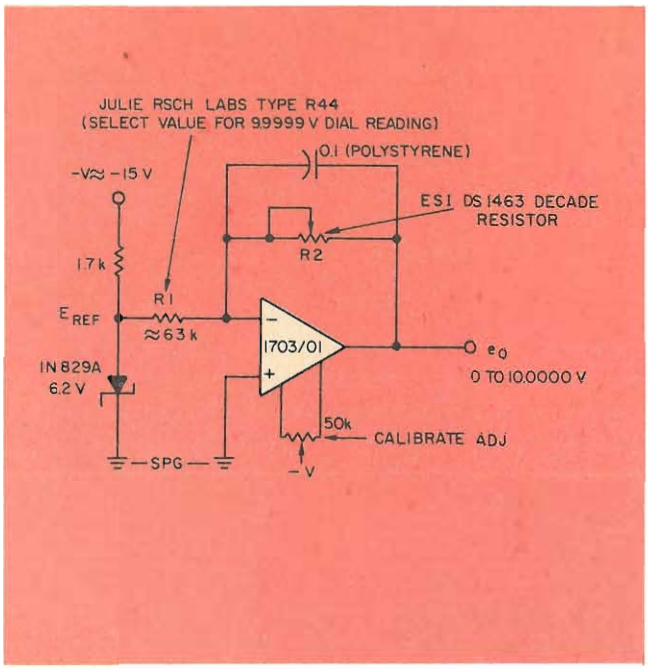
Even mixing resistor brands is an invitation to trouble.

Capacitors are often overlooked as sources of trouble in dc circuits. When they are used as bandwidth-limiting elements in feedback circuits, make sure their leakage doesn't add another error. An integrator's leakage is obviously critical—but so is "soakage," which is a measure of a capacitor's ability to charge or discharge without voltage lag or "leftovers."

A look at amplifier performance

So far we've seen many of the troublesome items that tend to be overlooked. Now let's examine the amplifier itself.

Carrier-modulated amplifiers, despite their impressive specifications, are not a solution to every measurement problem. Most chopper-stabilized amplifiers, for example, are limited in application because of their single-ended input; high-stability, differential-input op amps can



4. **Chopper-stabilized amplifiers** also form very stable voltage references. These are as stable as the zener diode used for the reference source.

more readily perform differential measurements. However, the common-mode rejection-ratio error can swamp out the amplifier's low drift. For applications where common-mode voltages are low, the differential-input amplifier is a good choice, but when common-mode voltages are high, use a chopper-stabilized amplifier with a pseudo-differential input (Fig. 3).

Chopper amplifiers have initial offset voltages down in the 10-to-20-μV region, while most premium FET or bipolar op amps have offsets in the hundreds of microvolts. And, unlike other amplifiers, choppers can be trimmed for offset without affecting $V_{os}/\Delta T_c$. This permits the amplifier's offset adjustment to be used as a calibration tweak (Fig. 4) or bucking adjustment.

High-performance op amps can come close to matching a chopper's offset temperature drift but not to equaling the chopper's power-supply rejection or time drift. All amplifiers take a "random walk" when it comes to offset voltage vs time. A differential amp may drift a few microvolts a month, but a chopper can achieve a low 5-μV-a-year offset drift. With unattended equipment, time drift can be critical.

Chopper-amplifier input bias current is usually about 50 pA, while FET input amplifiers go down to 1 pA and still maintain a 1 μV/°C offset tempco. Some FET op amps can even bias down to 0.1 pA, but at this low current you trade away offset stability. Remember, FET bias current doubles with every 10-C increase.

When bias current is the critical spec, look into the varactor-input amplifier with its femto-ampere bias currents. Varactors also have high common-mode rejection—even at 100 V. Their dc drifts (10 μV/°C) are relatively poor, and their bandwidth is low (typically 40 Hz or so).

When you make a choice, don't forget to consider possible interference from residual noise in chopper-amplifier outputs, open-loop gain (choppers have typical gains of 10^7 to 10^8 vs 10^6 for differential amplifiers), power consumption and price. Generally chopped amplifiers cost a bit more than differential-input units, and FET input differentials usually cost more than bipolar-input amplifiers.

Measure some key specifications

Some of the key specifications of carrier-modulated amplifiers—or any amplifier—can be verified by a few simple tests. Measure the offset voltage and its drift vs temperature. The test set in Fig. 5a allows these measurements to be taken. Set the amplifier up for a gain of 10,000, ground the input (with S_1 open), and you get the following offset vs output relationship:

$$E_{os} = \frac{E_o}{1 + R_2/R_1}$$

The gain of 10,000 allows most instrumentation to display the 10-to-20-μV offset voltage of the amplifier without any problem. If S_1 is closed and the potentiometer is adjusted to null the offset, $V_{os}/\Delta T$ can be established. With the initial offset nulled at 25 C, place the amplifier in a controlled 70-C environment and allow enough time for the amplifier to settle. Now measure the output voltage. Next, place the amplifier in a 0-C environment and measure the settled output voltage.

The offset-vs-temperature characteristic can be calculated from the standard "butterfly" equation:

$$E_{os}/T = \frac{E_{os}/70\ C}{70 - 25\ C} \text{ or } \frac{E_{os}/0\ C}{0 - 25\ C}.$$

Stable resistors and a well-constructed test jig (good grounding, shielding, etc.) will ensure accurate results.

Time drift, measured in microvolts/year, can also be extrapolated from the same test circuit, if the amplifier is held at a constant temperature (about ±0.1 C) for one day. The long-term error can then be calculated from

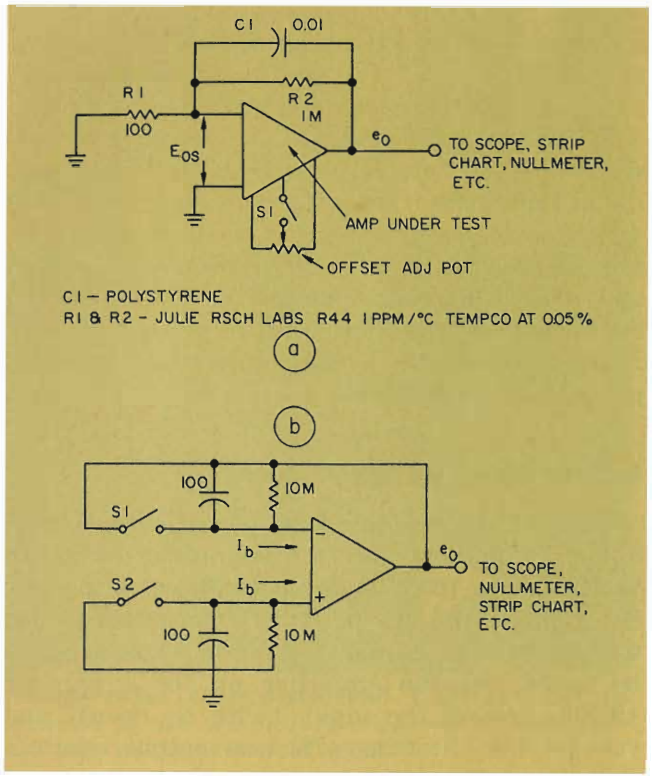
$$\Delta_{os}\ (1\ year) = \Delta_{os}\ (1\ day)\ (\sqrt{365\ days/year}).$$

Another circuit (Fig. 5b) can be used to determine the amplifier's input bias current. With S_1 or S_2 closed, the output voltage is related to the bias current at the appropriate input by

$$I_b = E_o/10\ M\Omega.$$

Temperature dependence can be measured in the same way as for offset voltage.

Once you have narrowed the choice to a specific



5. **A simple test jig** to check the amplifier for offset drift (a) or input bias current (b) doesn't require too many extra components.

amplifier type, the worst is over. Let's take a look at some applications of high-stability amplifiers.

Look at some circuit examples

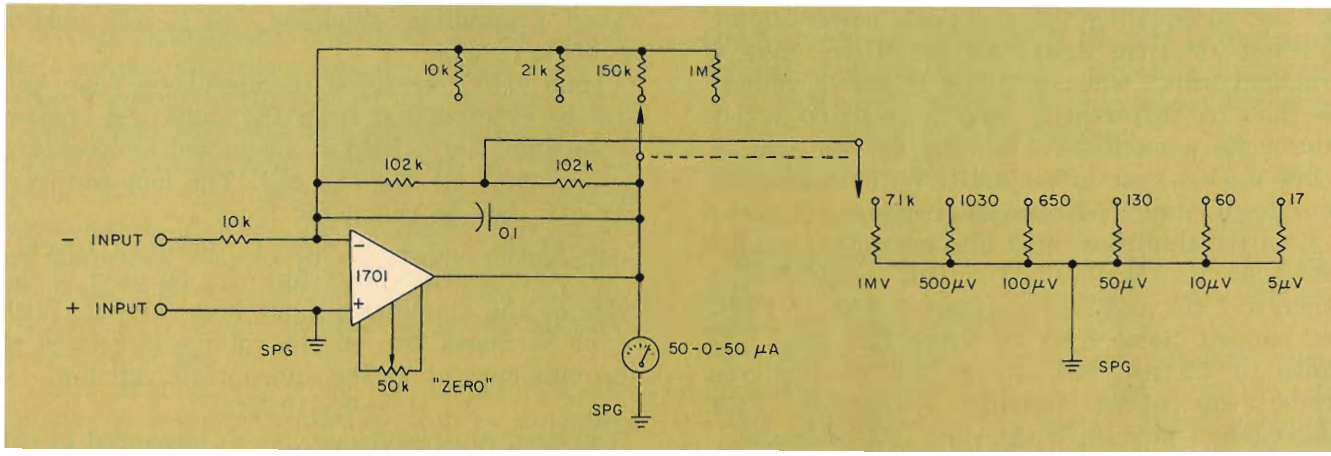
A null voltmeter/data amplifier with a 5-μV full scale sensitivity can be built with a bandwidth limited to only a few hertz if you place a 0.1-μF capacitor across the input and output terminals of the amplifier (Fig. 6). An external resistor switching circuit lets the modular amplifier cover many gain ranges. On the four lower-gain ranges, two 102-kΩ resistors parallel the switch-selected feedback values. On the higher sensitivity ranges, the feedback is divided by a ratio determined by the range switch value and the 102-kΩ resistor connected to the amplifier output. This compound T provides high gain without large feedback values, which in turn reduces leakage.

In this example the amplifier delivers an output to a meter, and thus the gain accuracy (as opposed to stability) need not be better than 1%. Metal-film RN60C resistors provide both good accuracy and low noise at reasonable cost. Since a typical meter movement might require only 100 μA, worst case, total quiescent current is only $\pm$3 mA from typical supplies. This circuit is handy for portable equipment.

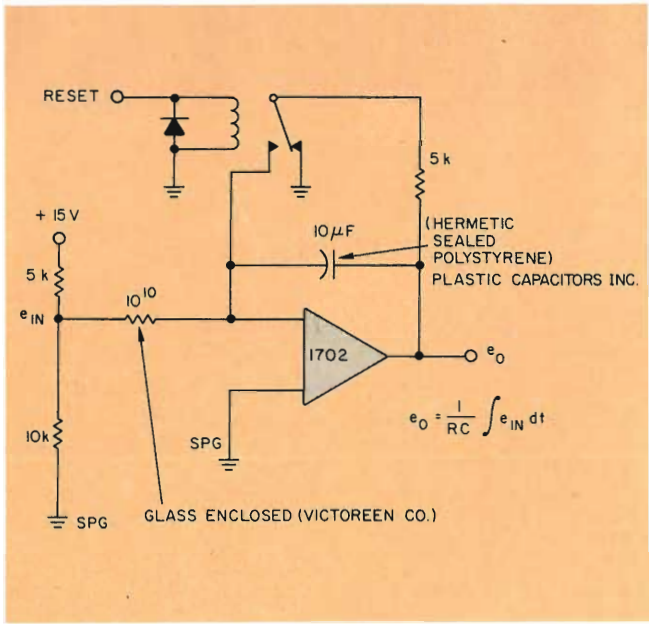
Single-ended instrumentation amplifiers can be used in differential measurement applications—just float the input in a bridge circuit (Fig. 3). This type of circuit not only permits the amplifier to extract the offset signal but, more significantly, completely eliminates the common-mode error of the differential amplifier. Even when an amplifier has a CMRR of 120 dB, the common-mode error can overshadow the input drift characteristics of a good differential amplifier. This capability is exploited by the temperature servo circuit of Fig. 2.

In this circuit the chopper's low bias current, low drift and high loop gain combine in a temperature-control system with very high performance. The true differential signal, derived from the bridge, is amplified to drive a Darlington-connected transistor pair. Thermal feedback from the heater and bridge thermistor produced a changing signal that the amplifier conditions. The potentiometer, in parallel with the heater element, should be adjusted to provide just enough feedback to prevent the main (thermal) loop from oscillating due to thermal delay.

This type of temperature-control circuit can



6. **Band-limiting of a null voltmeter** is easily accomplished if a 0.1-μF capacitor is placed across the input and output terminals to pass the high frequencies. This circuit has a 5 μV sensitivity.



7. **A long-time-constant integrator** can be formed if a high-quality capacitor is placed across a varactor input amplifier. In this case the time constant is extremely long—100,000 seconds.

hold to within microdegrees at a 50-C set point. And two such controlled ovens, one inside the other, can provide stability limited only by the thermal noise of the inner oven control thermistor.

Generate precision voltages, too

High-stability chopper amplifiers can also be used to generate precision output voltages that span six decades (Fig. 4). The output voltage from the circuit is based upon the stability of an external reference that feeds the inverting amplifier. The simple op-amp gain equation details the operation:

$$E_o = -(R_2/R_1)\, e_{ref}.$$

From this, you can see that if R_1 is carefully selected, the output voltage will be numerically identical to R_2. Thus if a multidecade precision potentiometer is used as R_2, any output voltage from 0 to 10 V can be dialed in.

Unlike direct coupled designs, a chopper-stabilized amplifier's offset tempco is independent of the offset voltage. Thus the offset potentiometer can be used as a calibration adjustment instead of a trim. The zener diode used should have a low tempco—typically 30 μV/°C or lower, since it directly determines the output stability.

The total worst-case error over a year's time under lab conditions (20 to 30 C) can be found from the following:

Diode thermal error
= (30 μV/C) (1.6 amp gain) (±5 C) = 240 μV.
Diode time error
= (60 μV/year) (1.6 amp gain) = 96 μV
total = 336 μV.
Amp thermal error
= (0.25 μV) (1.6 amp gain) (±5 C) = 2 μV.
Amp time error
= (5 μV/year) (1.6 amp gain) = 8 μV
total = 10 μV.
Resistor error = 1 ppm/year = 10 μV
total circuit error = 356 μV.

At 10 V full scale, that represents about a 36-ppm error, of which only 1 ppm comes from the amplifier. Zener drifts can be reduced, but the diode would still be the main error source. Thus you can reasonably expect one-year calibration intervals on an instrument that has a five-decade range.

Varactor bridge amplifiers, although not chopped, have many precision uses because of their low input bias current—about 2 fA. Only 20,000 electrons per second flow through the input of varactor amplifiers. A typical application is shown in Fig. 7, a circuit for a geophysics experiment in which a linear ramp must be generated over a 24-hour period with a maximum of 10 V.

On the ramp there are not to be any discontinuities or steps—which rules out the use of a digital-to-analog converter to form the output. The circuit acts as an integrator with a 100,000-second time constant and an accuracy that approaches 0.2%. Since the integrating resistor is 10^{10} Ω, the current available to charge the capacitor, bias the amplifier and deal with the capacitor's leakage current is given by

$$I = 10/10^{10} = 1 \text{ nA}.$$

If the capacitor has a leakage resistance of 10^{12} Ω, it will steal 10 pA of current from the input bias.

This leaves 990 pA to charge the capacitor and bias the amplifier. Since the current required by the amplifier is only 2 fA, its current drain doesn't really affect any error calculation. The capacitor's leakage, though, is the dominant error source. Humidity, radio waves, leakage paths and other interference can easily subvert the operation of this sensitive circuit.

To protect the amplifier and keep the accuracy high, the following precautions should be taken: Use a Teflon circuit board. Guard the input paths. Employ point-grounding techniques. And set up a sealed, shielded enclosure. ■■

Bibliography

Graeme, J. G., Tobey, G. E., Huelsman, L. P., "Operational Amplifiers: Design and Application," McGraw-Hill, 1972.

Patstone, Walter, "Designing Femtoampere Circuits Requires Special Considerations," *EDN*, July 1, 1972, pp. 34 to 36.

Williams, James, "Temperature Control to Microdegrees," October, 1971, paper available from MIT, Dept. of Nutrition and Food Science, Cambridge, MA.

Williams, James, "Split a Temperature Degree to 10 μ°C," *Electronic Design*, No. 10, May 10, 1974, pp. 110 to 113.

Float your input amplifier and you can almost laugh at ground loops or high common-mode voltages. A new design gives low drift, too.

Systems designers, take heart. The answer to your ground-loop headaches may lie in a novel isolation amplifier. Intended for high-accuracy dc applications, the amplifier has no trouble handling common-mode voltages as high at 600 V. And it drifts a wee 2 ppm/°C. All the amplifier asks in return is a scanty 200 nA of input bias.

Grounding is a paramount problem in many data-acquisition and process-control systems. Since transducers are often located hundreds of feet from an electronics console or computer, ground loops are hard to avoid.

For example, if a minicomputer is interfaced to a nuclear reactor located 1000 feet away, it is likely that the two equipments' grounds will not be at the same potential. Simply tying all the grounds together with heavy cable may not solve the problem. One possible solution is to float the computer or reactor off ground, but this may not be practical or safe.

Special types of amplifiers address this problem, with varying degrees of success. "Instrumentation" amplifiers, with committed feedback networks, provide high common-mode rejection ratios and excellent dc characteristics. These amplifiers achieve good results at moderate common-mode voltages. High common-mode voltages, however, call for an isolation amplifier with fully floated inputs.

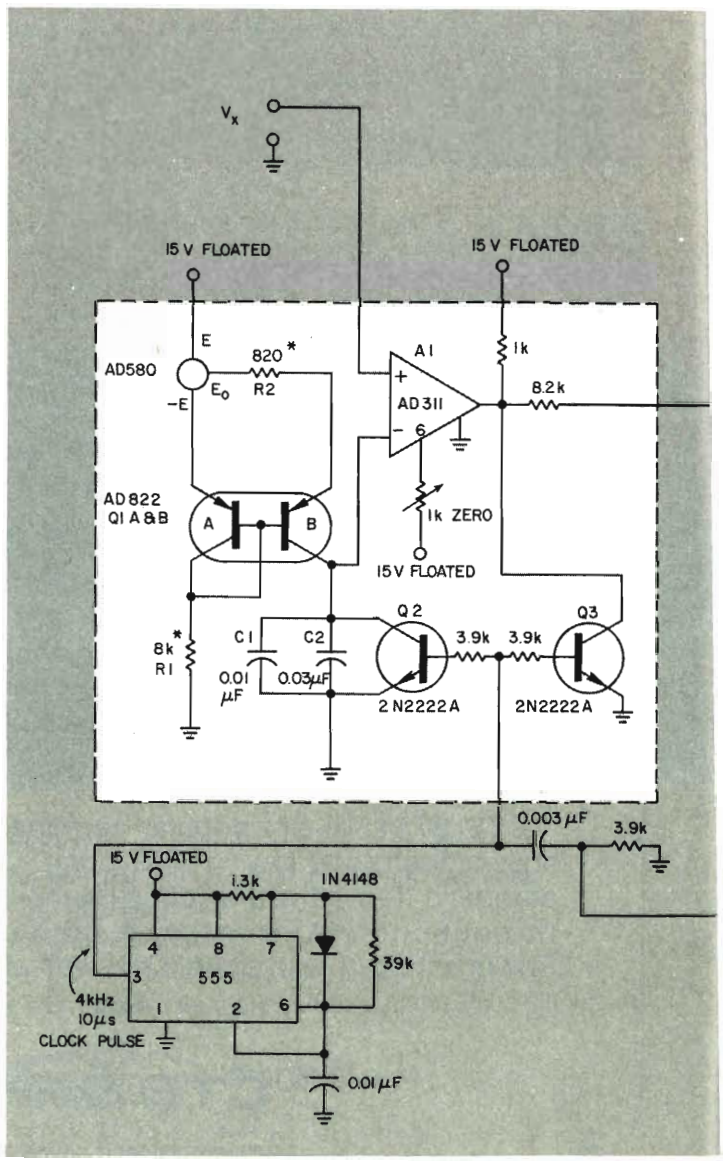
The basic principle

The design presented here achieves a precise unity-gain, input-output relationship for a 0-to-9-V input. Although there's no dc connection between input and output, the output follows the input to an absolute accuracy of 0.01% over a 0-to-50-C temperature range.

Commercially available isolation amplifiers, such as the Analog Devices 285L, can equal or surpass these specs, but do not approach the 2-ppm/°C drift performance.

Conceptually, the design is simple (Fig. 1). The input voltage is converted to a pulse whose width ranges from 0 to 90 μs. For isolation, the pulse is driven across a transformer whose secondary is referenced to output ground. The data pulse out of the secondary is demodulated by a pulse-width-to-voltage converter to form the amplifier output.

To convert the input voltage to a pulse width, the circuit compares the input with a precision linear-reference ramp that repeats at a rate of



James M. Williams, Senior Engineer, MIT, Dept. of Nutrition and Food Science, Cambridge, MA 02139.

4 kHz. The ramp runs from 0 to 10 V, then is reset to zero by a 4-kHz clock pulse. The output pulse width of the comparator depends on the time the reference ramp takes to slew from zero to the value of the input voltage, V_x.

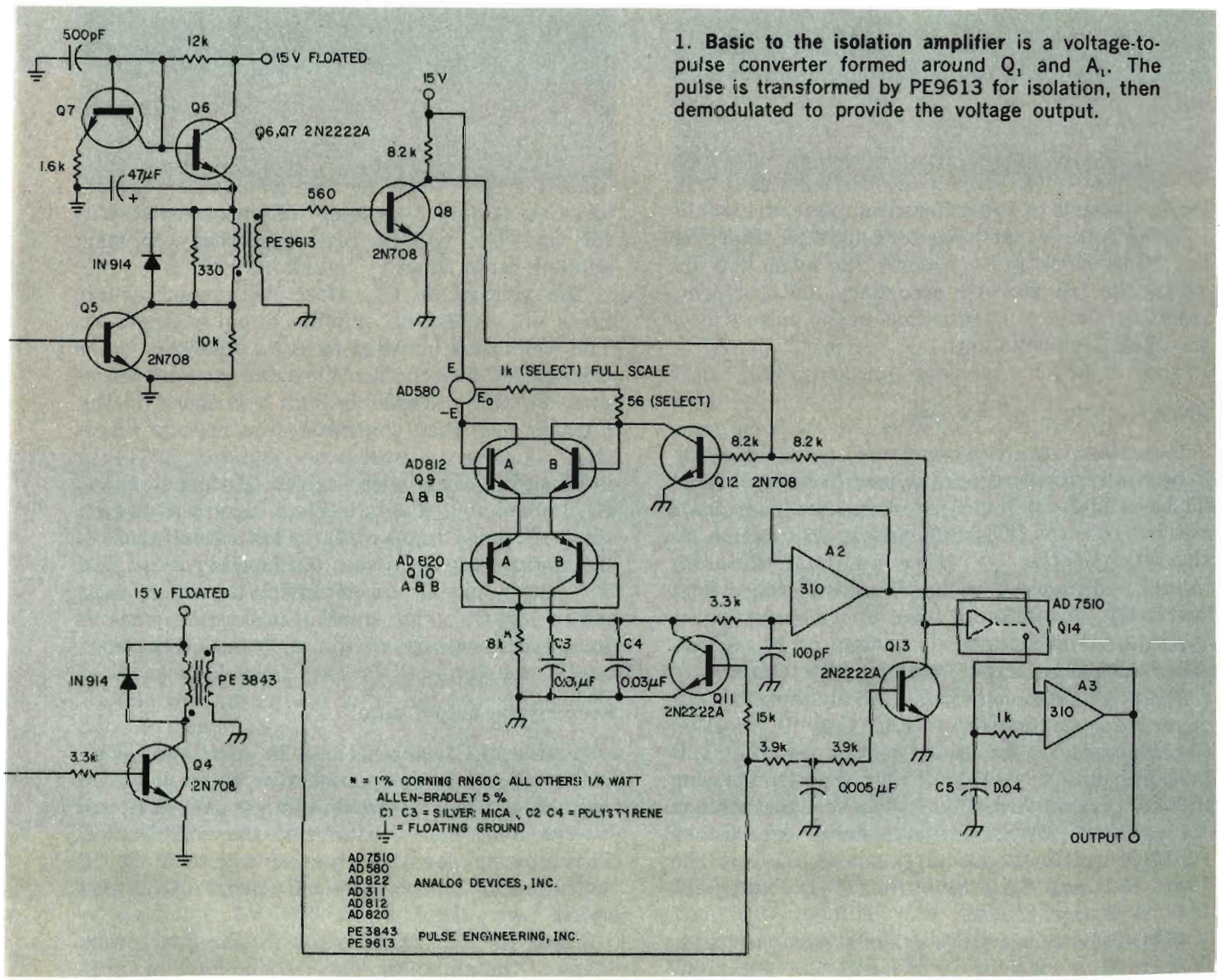
The secondary of the transformer reproduces the data pulse and uses the pulse to turn on a switchable ramp generator. The ramp starts at 0 V and goes toward 10 V until the data pulse goes low. At that point, the current source stops charging the ramp capacitor, and the voltage across the capacitor equals V_x, which is sampled and stored in another capacitor. The clock pulse resets the system, and the entire cycle repeats.

The detailed amplifier

In Fig. 1, transistor pair Q_1, comparator A_1 and associated components form the voltage-to-pulse converter. The AD580 (from Analog Devices) in the emitter of Q_1 is a band-gap voltage reference that stabilizes the differential pair in a current-source configuration. The "B" side of the pair functions as a current source, while the "A" side is diode-connected to compensate for the drift of V_{be}.

Resistors R_1 (8 kΩ) and R_2 (820 Ω) bias the current source to provide 6 mA into the $C_{1,2}$ combination. Because the tempcos of silver mica and polystyrene-type dielectrics are opposite, C_1 and C_2 form a capacitor with a zero-temperature coefficient and low soakage. The composite capacitor resets when the clock pulse from the 555 timer resets Q_2. The pulse is 10 μs long and repeats at a 4-kHz rate (Fig. 2a).

When the clock goes high, Q_2 turns on and $C_{1,2}$ resets to zero volts. When the clock goes low, Q_2 goes off and $C_{1,2}$ is charged up (Fig. 2b). The resulting repetitive, linear reference ramp forms the input to the AD311 comparator. The 6-mA charging current ensures that the comparator's input-bias current doesn't affect the linearity of



1. Basic to the isolation amplifier is a voltage-to-pulse converter formed around Q_1 and A_1. The pulse is transformed by PE9613 for isolation, then demodulated to provide the voltage output.

the reference ramp.

Voltage V_x serves as the other input to the AD311. Like the rest of the circuitry in the front end of the amplifier, V_x is referenced to floating ground. The pulse width at the output of the AD311, which is directly proportional to V_x, drives Q_5 into conduction (Fig. 2c). The collector of Q_5 conducts current out of Q_6's emitter, and the current passes through the PE9613 transformer primary to ground (Fig. 2d).

To keep the transformer out of saturation, the Q_6, Q_7 combination drives the transformer from a 1.2-V potential. Transistors Q_6 and Q_7 function as a temperature-compensated emitter follower, biased by the 12-kΩ and 1.6-kΩ resistors to provide about 1.2 V at Q_6's emitter.

The 500-pF capacitor ensures dynamic stability, and the 47-μF solid tantalum capacitor helps maintain a low impedance at Q_6's emitter when Q_6 is loaded (when Q_5 turns on). The 1N914 diode, 300-Ω and 10-kΩ resistors provide proper damping of the transformer primary. Transistor Q_5, a 2N708, has a low storage charge and provides very fast edges—even in the relatively slow common-emitter configuration.

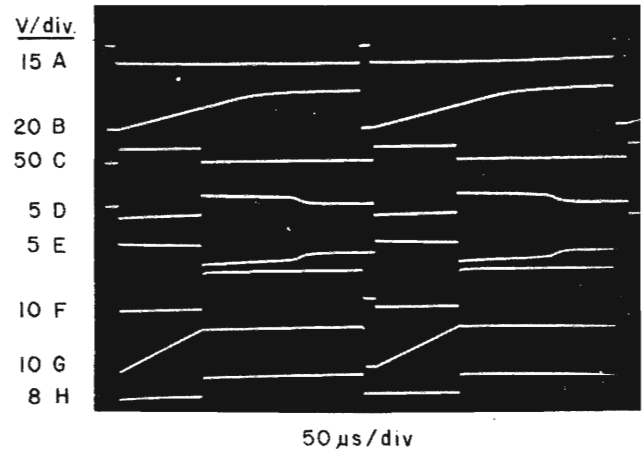
Transistor Q_3 is biased by the clock pulse and prevents the AD311 output from going high during the period that the clock pulse resets $C_{1,2}$. To do so, Q_3 pulls the AD311 output down when the clock pulse is high. The clock pulse biases Q_4 through the 0.003-μF/3.9-kΩ differentiator network. Because of the differentiator, Q_4 drives the PE3843 pulse transformer for only 3 μs whenever the 10-μs clock pulse occurs. The pulse appears across the transformer secondary and performs resetting and timing functions in the pulse-width-to-voltage demodulator.

Going back to a voltage level

Once the voltage-proportional pulse is established and driven across the transformer, it must be demodulated. The transformer secondary feeds current into Q_8 (Fig. 2e), which, in turn, shifts the level of the 1-V pulse and maintains the pulse's fast edges (Fig. 2f). Transistor Q_8's output drives Q_{12}, a switch that turns on a current source (AD812, AD820 transistor pairs) in 10 ns. Another AD580 reference stabilizes the source.

The "A" portion of the 820 functions as the current-source transistor, and the "B" portion provides temperature compensation. The AD812B pair prevents the AD820B pair from conducting in the reverse direction whenever the voltage across the C_3, C_4 composite capacitor exceeds the AD820B emitter potential (when Q_{12} is on). The 1-kΩ, 56-Ω and 8-kΩ resistors set the bias point for the current source.

Whenever a data pulse exists across the transformer, Q_8's collector is low and Q_{12} is cut off.



2. **Scope traces show the various circuit waveforms:** the 555 output—a 4-kHz, 10-μs pulse (A); the reference ramp at the comparator's negative input (B); the comparator output for V_x = 8 V (C); the transformer drive and secondary waveshapes (D and E); and the waveshape at Q_8's collector (F). The hop is caused by current sharing between Q_{12} and Q_{13}. Traces G and H show the voltage across $C_{3,4}$ and at the collector of Q_{13}, respectively. Note that the $C_{3,4}$ ramp starts when "F" is at 0 V.

The current source then charges $C_{3,4}$, which ramps up in voltage until Q_8 goes off and Q_{12} turns on. Thus, the current source is cut off very quickly (Fig. 2g).

Capacitor $C_{3,4}$ sits at the maximum ramp voltage until Q_{11} resets it to zero. Transistor Q_{11} is driven by the reset pulse from the transformer. Since the reset pulse for the demodulator capacitor, $C_{3,4}$, is only 3 μs long—as opposed to 10 μs for $C_{1,2}$—$C_{3,4}$ will be reset and ready to start another ramp when $C_{1,2}$ starts its ramp.

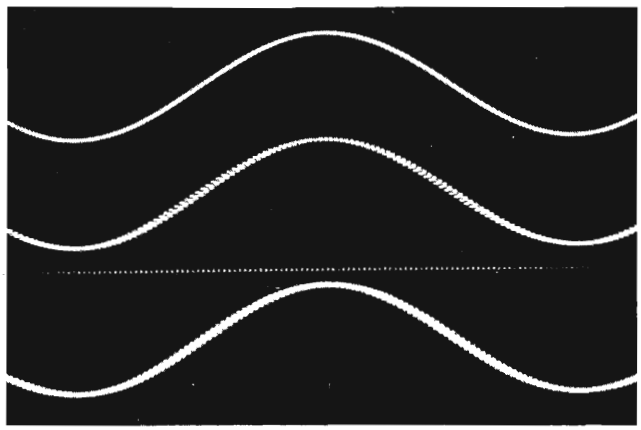
The voltage on $C_{3,4}$ after its current source turns off equals the amplifier-input voltage, V_x. This voltage is buffered by A_2, a follower, which drives FET switch Q_{14}. When the current source goes off, Q_8's collector is high and turns on Q_{14}. Capacitor C_5 then charges to the voltage across $C_{3,4}$.

When the clock pulse arrives, Q_{11} turns on, and $C_{3,4}$ immediately starts to reset to zero. However, the clock pulse biases on Q_{13}. This action turns off Q_{14}, and prevents C_5 from discharging (Fig. 2h). To ensure that Q_{14} is off during the entire reset period of $C_{3,4}$, the transformer reset pulse is stretched by the RC combination in Q_{13}'s base.

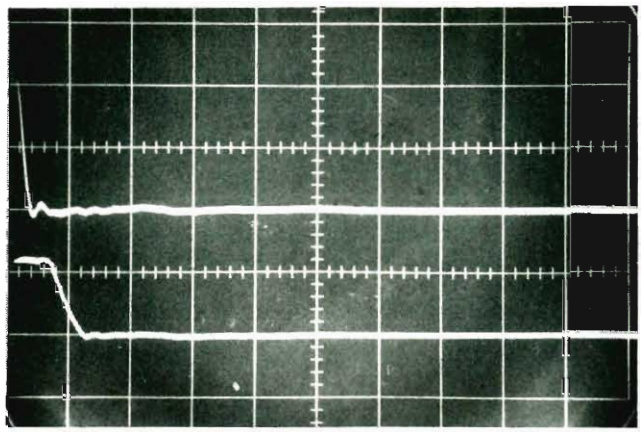
Keeping the output pure

Another RC combination—in A_2's input—provides a delay to compensate for Q_{14}'s slow 1-μs switching speed. Follower A_2's response is slowed by the 3-μs time constant of the combination. This slowing down further ensures that the resetting of $C_{3,4}$ doesn't affect C_5, despite Q_{14}'s slow speed.

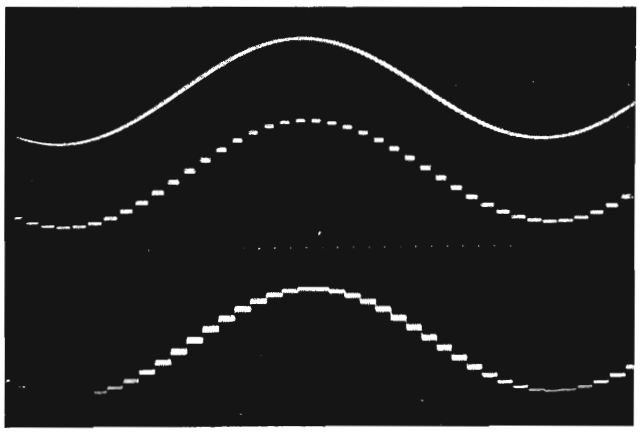
Capacitor C_5 is buffered by A_3, the final output stage of the amplifier. The 1-kΩ resistor in series



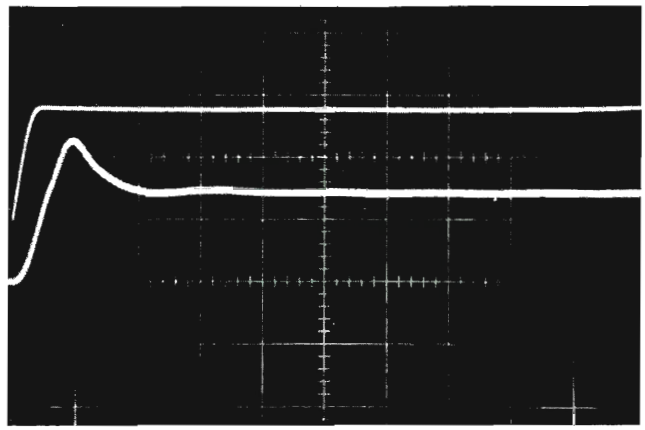
3. **The amplifier's response** to a 20-Hz sinusoid biased on a 2-V level (top). The center trace is the output of A_2, the bottom the output of A_3 (5 ms/div, 5 V/div).



5. **The fall-time delay** through transistor Q_5, transformer PE9613, and Q_8 and Q_{12} is measured at the AD311 output (top) and collector of Q_{12} (bottom).



4. **Response to a 200-Hz sinusoid:** The input is at the top, and the outputs of A_2 and A_3 are at center and bottom, respectively (625 μs, 10 V/div).



6. **Rise-time delay** is shown at the AD311's output (top) and at the collector of Q_{12} (bottom). The scope calibration here and in Fig. 5 is 500 ns and 5 V/div.

with A_3's input ensures dynamic stability.

All the provisions discussed ensure that only dc will appear at the amplifier's output for a dc input. Switching spikes and noise are below 1 mV. The amplifier's response is shown in Figs. 3 and 4, and the delays encountered through the circuit in Figs. 5 and 6.

To calibrate the circuit, apply 9.000 V at the input with respect to floating ground. Adjust the 1-kΩ in the AD812B collector line for 9.000 V at the amplifier output. Next, apply 10 mV at the input and adjust the 1-kΩ potentiometer at pin 6 of the AD311 for 10 mV at the amplifier output. Repeat this procedure until the adjustments do not interact.

Note that the offset adjustment (the 1-kΩ pot at A_1) is rather unorthodox—the method achieves a zero setting for the circuit by deliberately generating a large offset in the AD311 comparator. The adjustment is needed since V_{ce} saturation prevents Q_2 and Q_{11} from resetting their associated capacitors to zero. This "bending up" of the AD311's inputs increases bias current and E_{os} drift, but not enough to cause worry.

The 56-Ω carbon resistor in the AD812B collector line trims the entire circuit functionally to achieve the 2-ppm/°C drift. For example, the temperature drift of a standard Allen-Bradley 1/2-W resistor almost exactly compensates the residual-drift characteristics of the circuit from 0 to 50 C. Compensation results after slight changes in the charging current are delivered by the AD820-822 source to $C_{3,4}$.

The floating front end of the amplifier should be enclosed in a shielded metal box. If the circuit is exposed to moving air or sudden temperature transients, you can obtain optimum isothermal characteristics by putting the amplifier in epoxy resin.

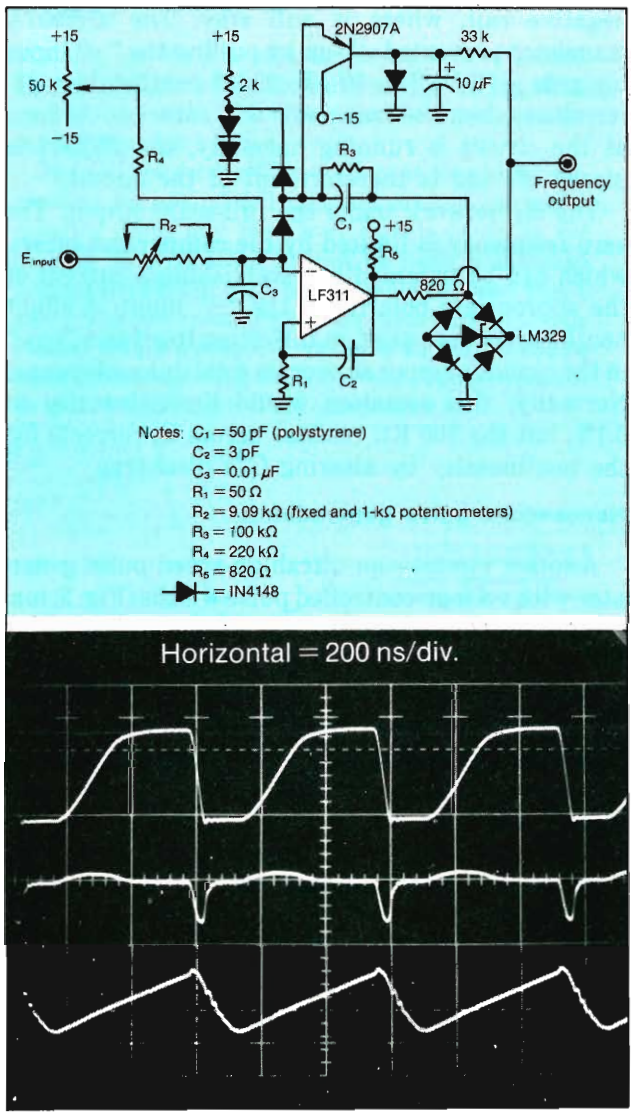
Some typical applications of the isolation amplifier include interfacing a remote computer to an instrument—without grounding problems; building a 500-V floating power supply with 0.01% regulation; and using the isolation amplifier after a chopper-stabilized preamp to obtain a composite amplifier with 100-nV/°C drift, a floating input and 0.01% absolute accuracy from 0 to 50 C. ■■

IC comparators carry speed and sensitivity at low cost into v-f converters: They team up with Schottky gates to generate nanosecond pulses, and they make highly linear pulse-width modulators.

IC comparators—at home in nearly any circuit

Excellent sensitivity, fast speed, and low cost make the IC comparator a formidable design element—it can be considered a nearly universal component. Because of its speed, it fits right into high-resolution voltage-to-frequency converters, establishing full-scale outputs as high as 2 MHz and a linearity as good as 0.06% down to 20 Hz. In an ultrahigh-speed mode, the IC comparator can team up with Schottky gates to generate nanosecond pulses or become part of a pulse-width modulator that boasts 0.05% linearity at repetition rates exceeding 250 kHz. With proper attention to bias currents, offsets, finite gain, slew-rate limitations, power-supply decoupling, and grounding, a designer can harness IC comparators to a seemingly limitless variety of applications (see "Adjusting the Comparator to High Performance") requiring digital pulse generators.

The v-f converter is one of the best applications for an IC comparator. In a simple 2-MHz v-f converter, the FET inputs of an LF311 comparator establish bias currents in the picoamp range and a linearity of 0.06% (Fig. 1, top). The LF311's output switches a capacitor, C_1, between a reference voltage and the comparator's negative input. The reference voltage is supplied by the LM329 diode bridge. The actual width of the output pulse is not important, so long as it lets the capacitor charge and discharge completely. The LF311 drives the R_1, C_2 combination, which provides regeneration feedback to reinforce the direction of "movement" of the amplifier's output. Positive feedback ceases when R_1, C_2's output decays. Any negative-going amplifier output is thereby followed by a positive edge after an amount of time governed by the R_1, C_2 time constant (top and middle waveforms, Fig. 1, bottom). The integration capacitor in the circuit, C_3 (a 0.01-μF unit), is



1. A 2-MHz voltage-to-frequency converter (top) can be constructed with the LF311 high-speed comparator. The associated waveforms (bottom) are governed by the charge-decay path through R_1, C_2. The topmost waveform on the scope photo is on a vertical scale of 20 V/div; the middle and bottom waveforms, on a scale of 0.5 V/div.

Jim Williams, Applications Manager
National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95051

never allowed to charge beyond 400 to 500 mV, because it is constantly reset by a charge "dispensed" from the switching of C_1 (bottom waveform).

Whenever the amplifier's output goes negative, C_1 dumps a quantity of charge into C_3, forcing it to a lower potential. The amplifier's negative-going output also transfers a short pulse through C_2 to the "+" input. When this negative pulse decays so that the "+" input is higher than the "−" input, C_1 can again receive a charge, and the entire process repeats. The diodes in C_1's path compensate the diodes in the bridge.

A word of caution: This circuit can lock up under several conditions. Allowing C_3 to charge beyond 400 to 500 mV (during start-up, overdrive at the input, etc.) will send the output of the amplifier to the negative rail, where it will stay. The 2N2907A transistor prevents lock-up by pulling the "−" input towards −15 V. The 10-μF, 33-kΩ combination determines when the transistor will come on. As long as the circuit is running normally, the 2N2907 is biased off and is therefore out of the circuit.

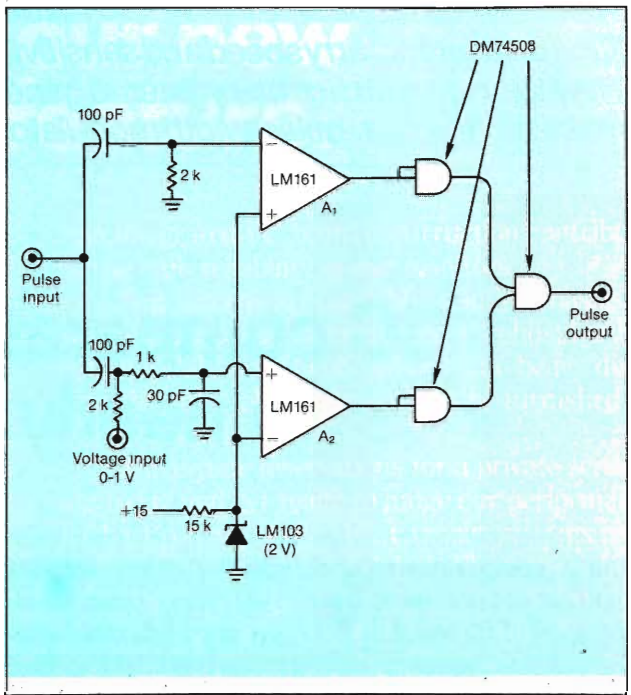
The R_2 network trims the full-scale output. The zero frequency is limited by the comparator offset, which can be trimmed by establishing a current of the appropriate polarity at the "−" input. A slight nonlinearity does exist, manifesting itself as a "bow" in the circuit's response over its total dynamic range. Normally, this situation would limit linearity to 0.1%, but the 100 KΩ resistor across C_1 corrects for the nonlinearity by altering C_1's discharge.

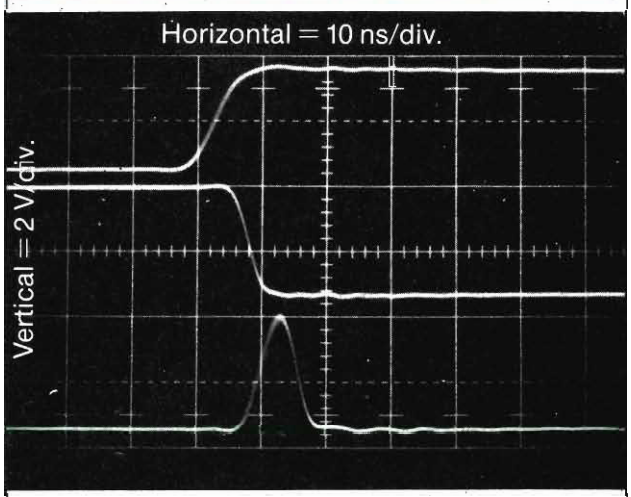
Nanosecond pulse generation

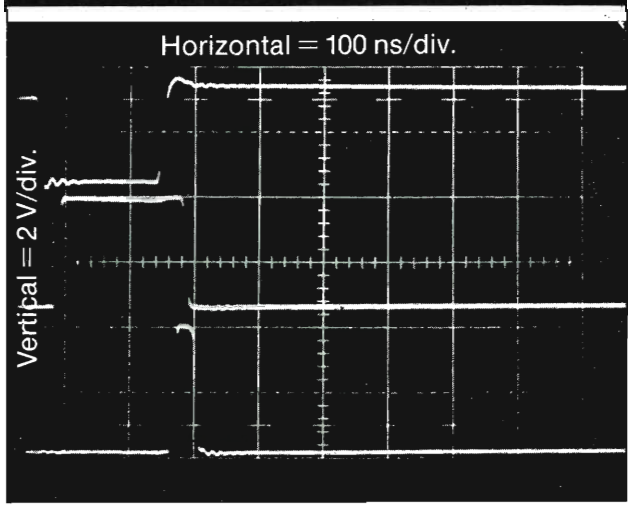
Another circuit—an ultrahigh-speed pulse generator with voltage-controlled pulse widths (Fig. 2, top)—demonstrates other virtues of the IC comparator. In this application, two differentiator networks generate two pulses, each with a distinct, controllable, duration. Ultrahigh-speed comparators and a DM74S08 Schottky gate extract the difference between the two pulse widths, and present it as a single high-speed pulse at the output.

Control voltages in the range of 0 to 1 V are applied at the input of the circuit to vary the pulse width from 0 to 100 ns. The switching speeds of the comparators and the gate limit the minimum obtainable pulse width to approximately 6 ns, with rise and fall times of about 2 ns.

As Fig. 2 (middle) suggests, with a control voltage of 100 mV, a composite pulse (having a 10-ns pulse width) can be generated in less than 20 ns. (The top trace is the output voltage of comparator A_1, the second trace is the output of A_2, and the third trace is the composite pulse. The vertical scale for all three waveforms is 2 V/division, and the horizontal scale is 10 ns/division.)







2. A high-speed pulse generator relies on Schottky gates and two comparators (top). A 100-mV control voltage will generate a 10-ns pulse width (middle); 1-V will produce a 100-ns width (bottom).

A positive pulse applied at the input of the dual 1-kΩ, 100-pF differentiator network will create a positive step across comparators A_1 and A_2. When this positive-going step exceeds the 2-V threshold established by the LM103 zener, both comparators switch their output states. With the voltage-control input at 0 V, the differentiator networks normally respond at the same time, and the two comparator-output transitions show identical waveforms, at least initially. As the control voltage increases, however, the spike produced by A_2's differentiator will arrive at the 2-V threshold earlier than the output produced by A_1's differentiator.

The A_2 differentiator will also take longer to decay through the 2-V threshold. This action would normally cause A_2's output to switch earlier than A_1's and to remain high for a longer time. However, the 1-kΩ, 30-pF network at A_2's "+" input provides a delay, which phase-shifts A_2's output so that A_1's leading edge occurs first (top and middle waveforms, Fig. 2, bottom). Therefore, A_2's trailing edge occurs after A_1's trailing edge. The length of time between A_1's trailing edge and A_2's trailing edge will depend upon the control voltage applied. For the values shown, a 0 to 1-V control range will produce a pulse-width difference of 0 to 100 ns. The DM74508 Schottky gate extracts this difference and represents it as a single pulse at the circuit output.

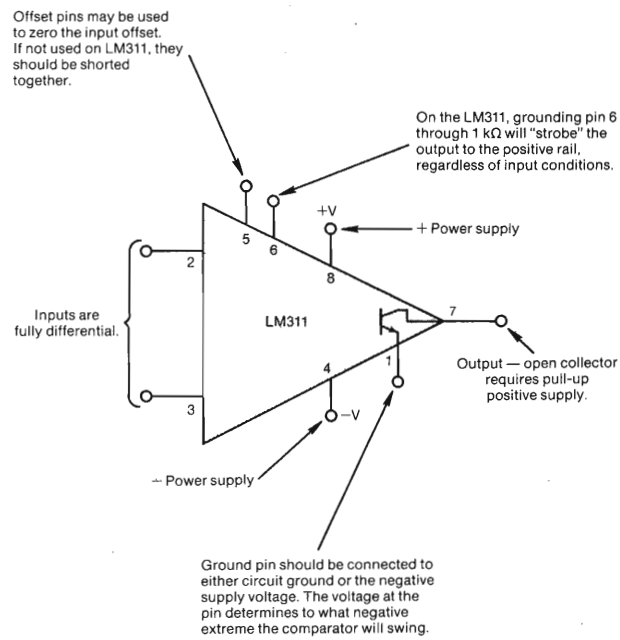
Adjusting the comparator to high performance

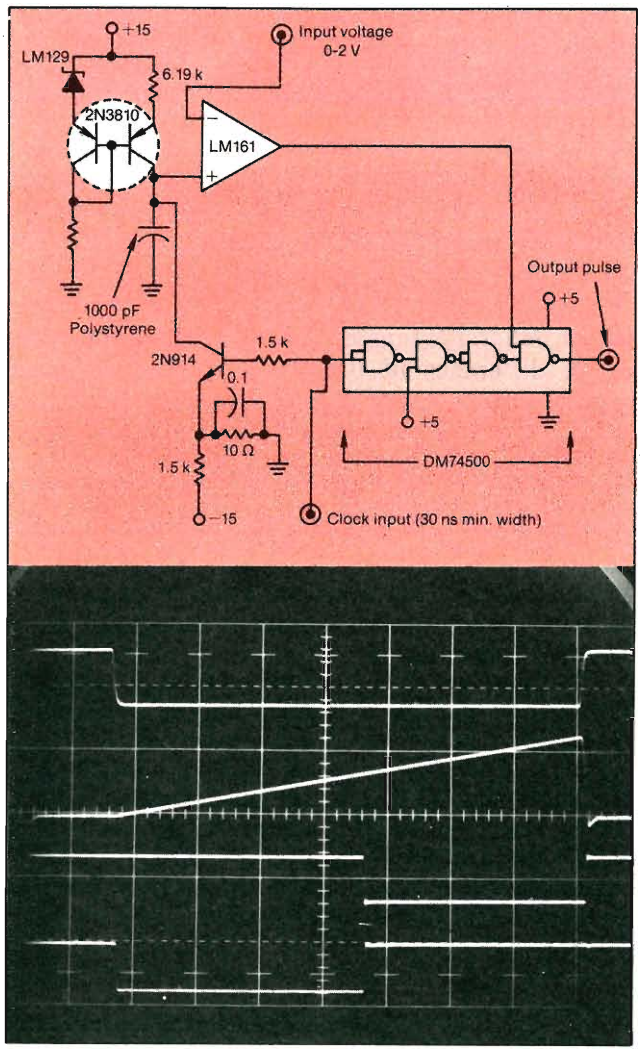
In the LM111/LM311 comparators, pins 5 and 6 are unnecessary auxiliary inputs and can be used for trimming adjustments. The trimmer should be placed within several inches of the comparator on the PC board. A 0.01-μF capacitor across pins 5 and 6 will minimize the comparator's susceptibility to ac coupling. A smaller capacitor is acceptable if pin 5 is used to pipe in positive feedback.

Certain sources will produce a cleaner comparator-output waveform if a 100 to 1000-pF capacitor is connected directly across the input pins. When the signal source is applied through a resistor, it is usually advantageous to place a resistor of substantially the same value in the other input both for dc and for dynamic (ac) considerations. Carbon, tin-oxide, and metal-film resistors have all been successfully designed into comparator input circuitry. Inductive wirewound resistors are not suitable.

When comparator circuits have input resistors (e.g., summing resistors), the value and placement of the resistors are particularly important. In all cases, the body of the resistor should be close to the device or socket, so that the leads or printed-circuit foil between the comparator and resistor can be kept too short to radiate or pick up signals. The same applies to capacitors, pots, and other components. For example, if source resistance equals 10 kΩ, as little as 5 in. of lead between the resistors and the input pins can produce oscillations that are very hard to damp. Twisting these input leads tightly is the only (but second best) alternative to placing resistors close to the comparator. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully, preferably with a groundplane under the circuitry (for example, on one side of a double-layer circuit card). Ground foil or either positive-supply or negative-supply foil should extend between the output and the inputs, to act as a guard.

The foil connections for the inputs should be surrounded by ground foil to guard against capacitive coupling from any high-level signals (such as the output). If a capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power-supply bypass capacitors should be located within a couple of inches of an LM111. (Some other comparators require the power-supply bypass to be located right next to the comparator.)





3. A linear pulse-width modulator (top) employs a discrete current source in addition to the LM161 high-speed comparator. Comparator switching—as shown in the accompanying waveforms (bottom)—is governed by the charging rate of the 1000-pF input capacitor. The first waveform is the clock, the second is the capacitor, the third is the comparator output, and the fourth is the output of the circuit. All waves are on a vertical scale of 5 V/div, except the capacitor at 2 V/div. The horizontal scale is 500 ns/div.

A somewhat slower, though highly linear, use of the LM161 is shown in Fig. 3 (top). Coupled with a discrete current source (the 2N3810) and a 1000-pF capacitor, the LM161 provides a 20-ns response to 30-ns pulses from an external clock. The circuit integrates within 3.5 μs for clean, precise modulation, with a typical linearity of 0.05% and a pulse-repetition rate better than 250 kHz.

The 2N3810 current source charges the 1000-pF capacitor. The voltage on the capacitor, rising in a linear fashion, is compared by the LM161 to the circuit-input voltage. The time required for the capacitor to charge to the circuit-input voltage will vary linearly with the value of that voltage. This time period can be represented as a pulse width at the output of the circuit.

The 2N914 resets the 1000-pF capacitor to zero when the external clock input goes high. The high clock input closes the DM74500 gates; moreover, no circuit output can appear until the clock input goes low. As soon as the clock goes low, the 2N914 turns off; the capacitor begins to charge (waveforms, Fig. 3, bottom), and the circuit output goes low. When the 1000-pF capacitor voltage crosses the circuit-input voltage, the LM161 switches and the circuit output goes high. This process is repeated for each clock pulse applied to the circuit.

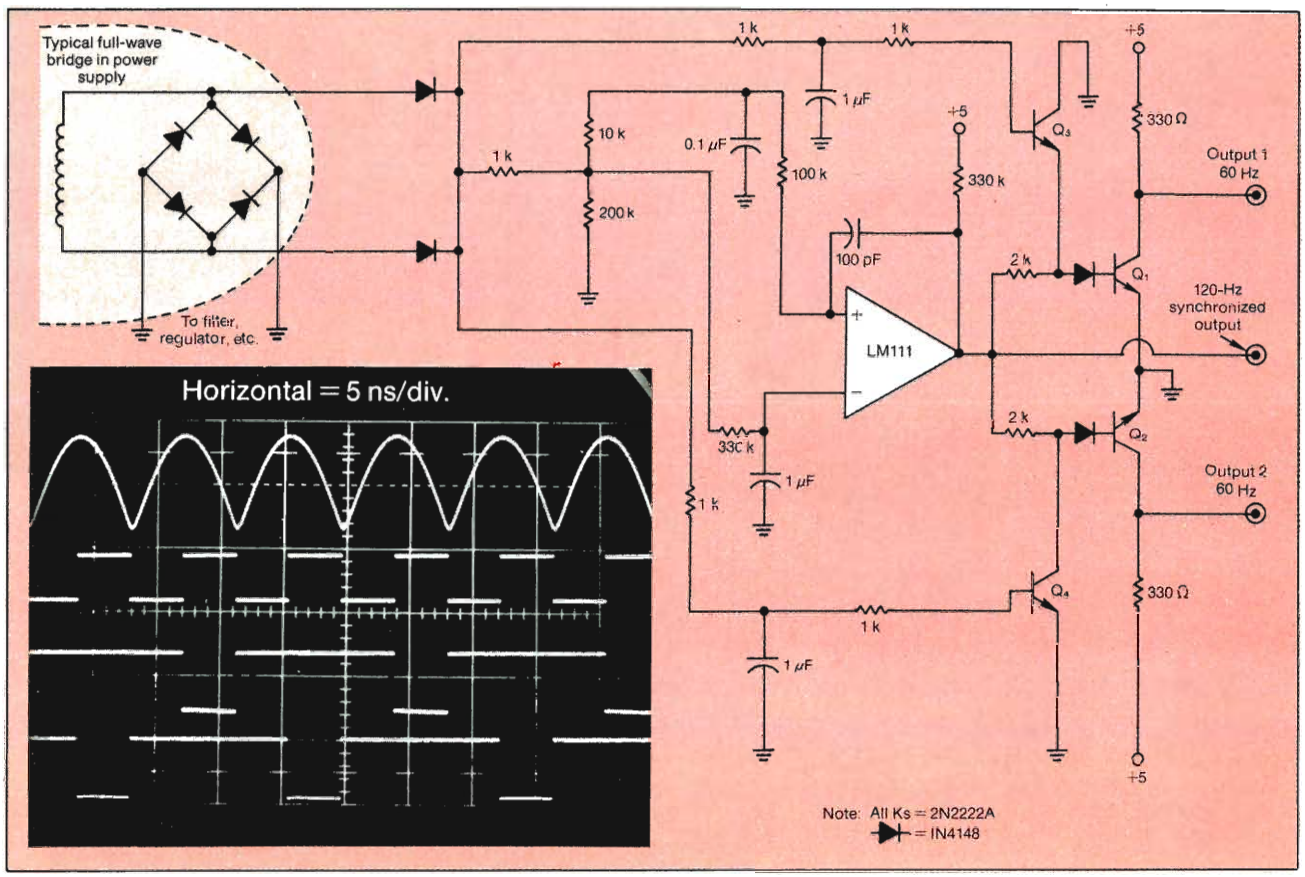
Components at the 2N914 ensure a true 0-V reset for the capacitor by providing a negative emitter potential equal to the V_{CE} saturation of the 2N914. The current source provides a ground-referenced output, making it easy to reset the capacitor.

Precision data converters

The resolution of inexpensive comparators, such as the LM311, can be improved as needed for analog-to-digital converters by boosting the compared input signals over a wider voltage range. An operational amplifier will bring enough gain and slew rate into the circuit to ensure that the comparator makes accurate comparisons at the 16-bit level. The output of the op amp remains high until the ramp voltage applied at one input of the circuit crosses the absolute value of the dc voltage at the other input.

While the op amp is high, the output of the LM311 comparator is low. (During this period, a diode bound in the feedback loop of the op amp prevents amplifier saturation and limits the output to 0.6 V.) However, when the ramp crosses the value of the dc voltage, the net current through the circuit's 22-kΩ input resistors balances precisely, and the op-amp output goes to 0 V.

As the ramp continues, the amplifier output goes to the negative side. The LM311 detects this zero crossing and switches its output. Feedback (ac) ensures a noiseless transition. Because the op amp



4. Line-synchronization circuits (top) can provide any number of synchronized 60 and 120-cycle outputs (bottom). All waveforms are on a vertical scale of 5 V/div, except for the first at 10 V/div. The horizontal scale is 5 ns/div.

operates at a gain of 15 during the zero crossing, the apparent slew rate of the ramp and the voltage difference between the two inputs is "expanded" by this factor, easing the comparator's job.

Line-synchronization circuits

Comparators can also be incorporated in 60-Hz line-synchronization circuits. The circuit in Fig. 4 (top) will operate from the full-wave bridge of almost any power supply and provide a synchronous 120-Hz output, as well as two 60-Hz outputs that occur on alternate cycles of the line. This capacity is useful in line-related noise-cancellation circuits, industrial data-acquisition and process-control systems, and especially in motor-control circuits.

The circuit runs on a single 5-V supply and uses an adaptive trigger threshold to maintain synchronization despite large changes in line voltage. The 60-Hz signal input is taken through two diodes, which are connected to the power supply's bridge rectifier. These diodes rectify the 60-Hz sine wave (top waveform in Fig. 4, bottom.) The resultant 120-Hz signal is divided down, so that the peak value falls within the LM111's common-mode voltage range. The "+" input of the LM111 is fed through the 10-kΩ, 0.1-μF filter for line-noise rejection. The LM111's "−" input receives the dc value of the 120-Hz waveform. The 330-kΩ, 1-μF values provide filtering. The voltage that sets the circuit's trigger point will vary directly with the line voltage. Under these input conditions, the LM111 output looks like the second waveform in Fig. 4 (bottom).

The LM111 output drives the circuit's output transistors (Q_1 and Q_2). Normally, these devices would provide identical inverted versions of the comparator output. In the circuit in Fig. 4, however, Q_3 and Q_4 function as synchronous demodulators at the output and are driven by the 120-Hz input waveform; moreover, they can turn on only when their respective modulating transistors are off (the third and fourth waveforms in Fig. 4, bottom, are the circuit output). The two outputs are, therefore, at 60 Hz and out of phase. The 1-kΩ units and the 1-μF capacitor, in each of the demodulator transistor's base lines, filter the line noise. Output transistor emitters are tied to ground.□

How useful?	Circle
Immediate design application	553
Within the next year	554
Not applicable	555

MDACs control frequency—not just amplitude—of signals

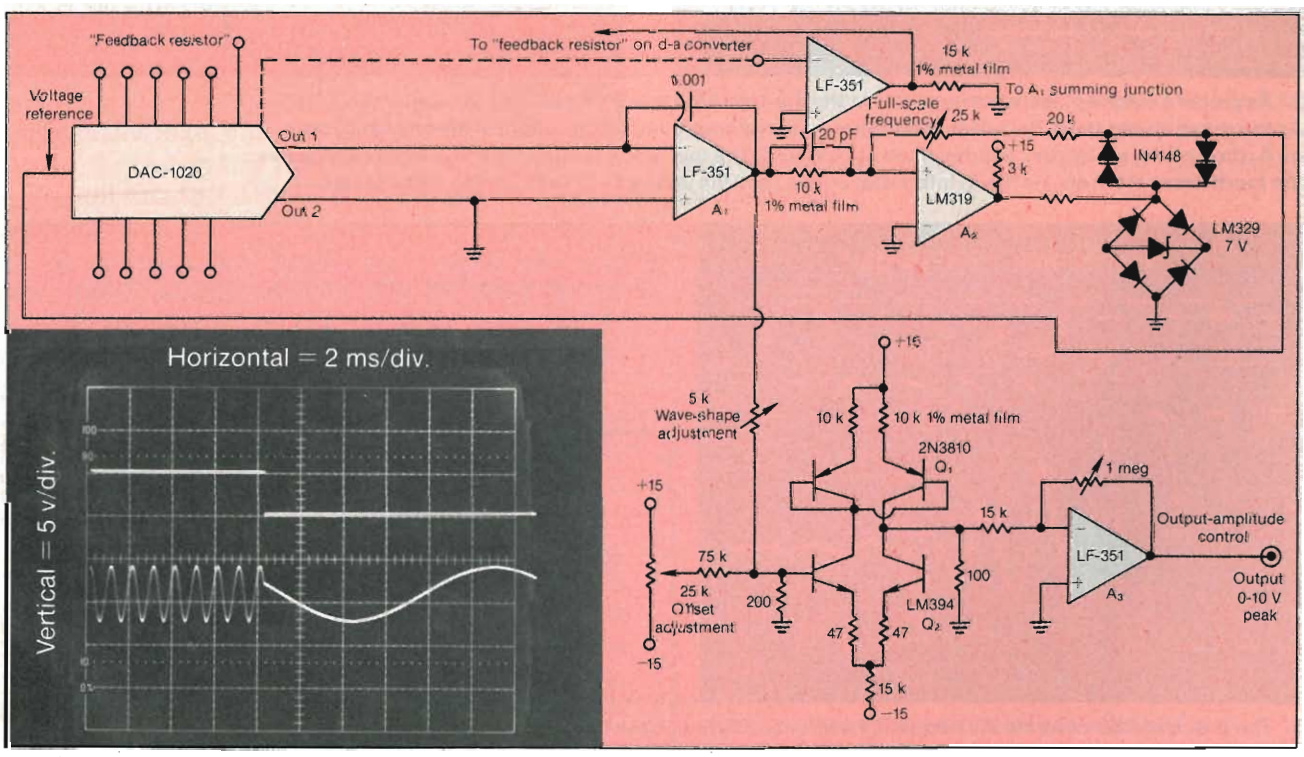
CMOS multiplying digital-to-analog converters can control the frequency of an analog signal as well as its amplitude. Especially in sine-wave generators, a 10-bit d-a converter can control up to 1024 discrete output frequencies, with a linearity better than 0.1%. This precise digital control is not merely inexpensive—it also provides better precision and repeatability than normally available from linear potentiometers, rotary switches, and other front-panel controls.

A CMOS multiplying d-a converter establishes control by accepting a wide range of digital inputs at its reference input. With a conventional converter, the reference input serves as the standard when analog signals are "assembled" from a variable digital input. In the multiplying mode, however, the digital input becomes the standard that controls a continuously variable analog input. Thus, the converter can control the amplitude of analog signals (in gain-control applications) and the scale factor of logarithmic amplifiers. Or, it can be harnessed to control the roll-off point of active filters, as well as the output frequency of sine-wave generator circuits.

In a sine-wave generator, with an output that varies from 0 to 30 kHz (Fig. 1, top), a 10-bit d-a converter generates 1024 discrete output frequencies. The linearity of the output signal to the digital code is within 0.1% and the response time is fast. As shown in Fig. 1 (bottom), the generator's output (first trace) changes rapidly in response to the digital word (second trace).

The d-a converter pulls current from the summing junction of integrator A_1; the amount of current is proportional to the digital code. A triangular waveform results from ramping up A_1 until the potential at A_2 changes state. With the output of A_2 feeding back into the reference input of the d-a converter, every change of state at the summing junction of A_1 will cause the 7-V potential at the reference input to change from plus to minus.

Jim Williams, Applications Manager
National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95051



1. A 10-bit d-a converter can generate 1024 discrete frequencies with a linearity of 0.1% in a variable-frequency sine-wave generator (top). The traces (bottom) show the rapid change of the generator's output (bottom trace) in response to the digital word (top trace).

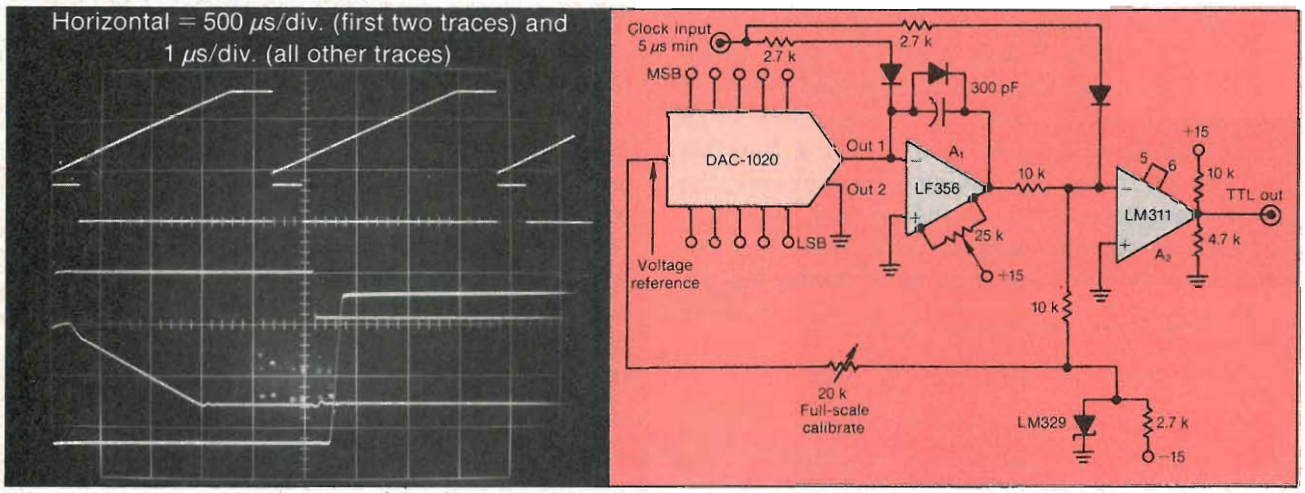
Moreover, the d-a converter will pull current in the opposite direction. The frequency of the amplitude-stabilized triangular waveform depends on the digital word at the d-a converter.

A 20-pF capacitor after the summing junction of A_1 improves the linearity of the generator at higher frequencies by providing a leading response to the 20-ns response of A_2. The four-transistor shaper network produces the sine-wave output by using the logarithmic relationship between V_{BE} and the collector current to smooth the triangular waveform. A 25-kΩ potentiometer fixes the output of the generator by setting all d-a inputs high and adjusting for a 30-kHz output; a distortion analyzer is used to adjust the 5-kΩ and 75-kΩ potentiometers in the shaper network for minimum distortion at the output. Over changes in temperature, the absolute change in resistance in the d-a converter's ladder network may cause unacceptable errors. This situation can be counteracted by reversing A_2's inputs and inserting an amplifier (dashed lines in schematic) between the d-a converter and A_1. Because this amplifier uses the d-a converter's internal feedback resistor, the temperature error in the ladder is cancelled and more stable operation results.

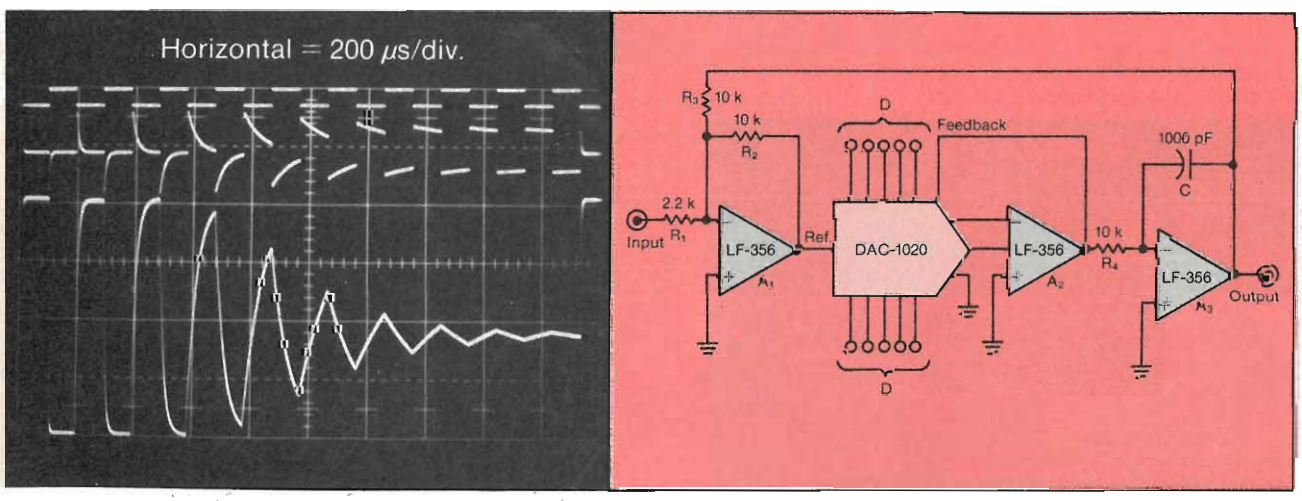
Pulse-width modulator control

In controlling the width of externally applied pulses, a 10-bit d-a can once again provide up to 1024 discrete pulse widths, with 0.1% linear conformance to the digital code.

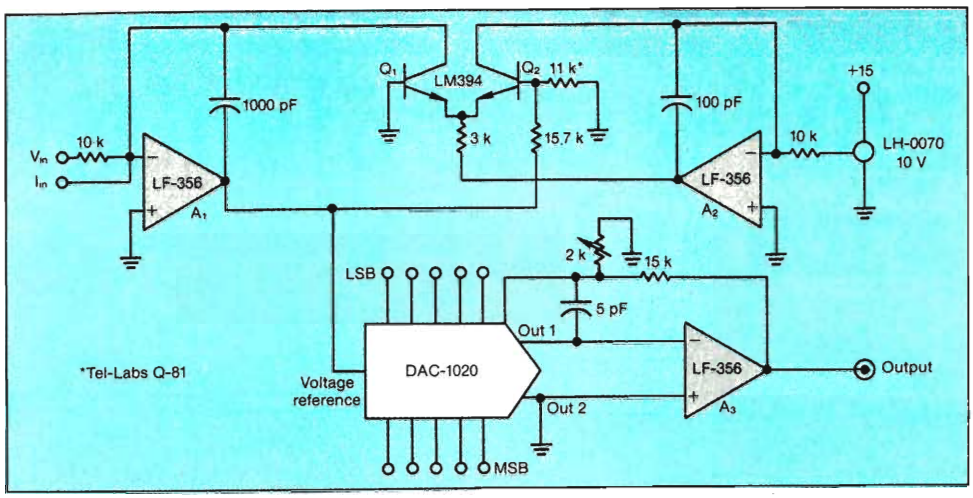
For a simple pulse-width modulator (Fig. 2, right),



2. As part of a simple pulse-width modulator, the d-a converter again establishes a linearity of 0.1% (right). As the graph shows (left), the width of the input pulses is controlled by the length of the charging ramp on A_1 (first trace, at 10V/div.; second trace at 20 V/div.). The third trace (5 V/div.) is a 5-μs input clock pulse; the fourth trace (10 V/div.) is the A_1 integrator output; and the last trace (5 V/div.) is the output pulse.



3. The d-a converter controls the frequency response of a high-pass filter by varying the time constant of the A_3 integer (right). The traces show how the cutoff frequency of the circuit decays as the decoder shifts a 1 through the d-a converter (left). The first trace (10 V/div.) is the input waveform; the second trace (20 V/div.) is the output of A_1 and the reference input of the d-a converter; and the third trace (0.5 V/div.) is the output of the circuit from A_3.



4. The conversion from a linear to log scale in a logarithmic amplifier is handled by Q_1, with compensation by Q_2 and the 1-kΩ resistor. The digital code on the d-a converter then settles the scale factor.

the ramp current on integrator A_1 is controlled by the digital code. While the ramp current is building, the output of comparator A_2 remains high. Once the voltage from the integrator is high enough to trip the comparator, the comparator output goes low. In this manner, the width of the input pulses is controlled by the length of the charging ramp on A_1 (Fig. 2, left, first and second trace).

In Fig. 2 (left) the third trace is that of a 5-μs input clock pulse, and the fourth trace is the A_1 integrator output. During the time the clock pulse is high, the current through the 2.7-kΩ resistor and diode path keeps A_2's output low. When the clock pulse goes low, the comparator's output goes high and remains high, until the A_1 integrator once again ramps up to the trip point.

To calibrate this circuit, all d-a converter bits are set high, and the 20-kΩ full-scale potentiometer is set for the maximum desired pulse width. The next adjustment, performed with only the least significant bit set high on the d-a converter, trims the A_1 offset potentiometer to provide a pulse width that is 1/1024th of the full-scale width.

Once again, temperature stability can be improved by substituting a FET switch for the clamp diode in A_1's feedback loop (which likely has a 2.2-mV/°C drift).

A multiplying d-a converter can precisely control high-pass filter networks by shifting the cut-off frequency in increments.[1] The d-a converter (Fig. 3, right) controls the frequency response of the filter by varying the time constant of the A_3 integrator. The relationship between the cut-off frequency and various circuit elements is given by

$$F_c = \frac{R_2}{R_3} \times \frac{D}{2\pi R_4 C},$$

where D is the digital increment (1 to 1024) of the d-a converter.

In Fig. 3 (left), a test circuit is driven by square-wave pulses while a 1-out-of-10 decoder shifts a ONE sequentially through the d-a converter's registers. As the decoder shifts the ONE towards the lower-order input of the d-a converter, the cut-off frequency of the circuit decays rapidly.

A multiplying d-a converter easily controls the gain of a linear amplifier; but setting the scale factor of a logarithmic amplifier (Fig. 4) can be more difficult. The actual conversion from linear to log scale is performed by Q_1, with compensation by Q_2 and the 1-kΩ resistor. With the log input applied to the reference input of the d-a converter, the digital code on the d-a converter will set the log scale of the amplifier.□

References

1. *Applications Guide to CMOS Multiplying D-a Converters*, Analog Devices, Inc., Norwood, MA, 1978.

IC instrumentation amp enhances transducer measurements

An IC instrumentation amplifier that surpasses the performance levels of virtually all others—regardless of construction technique or price—brings new levels of capability to measurement and control applications. Benefits include very low input offset drift and noise, stable gain setting, high common-mode rejection and differential, floating inputs. As a result, the LM163 gives the low-level signal outputs of strain-gauge bridges, RTD bridges, and other transducer elements the signal conditioning and amplification that count. Several applications will benefit, including high-accuracy barometers, thermocouple amplifiers and temperature-control circuits, high-voltage bridge drivers, and synchronous demodulators for extracting a modulated signal from a noisy carrier.

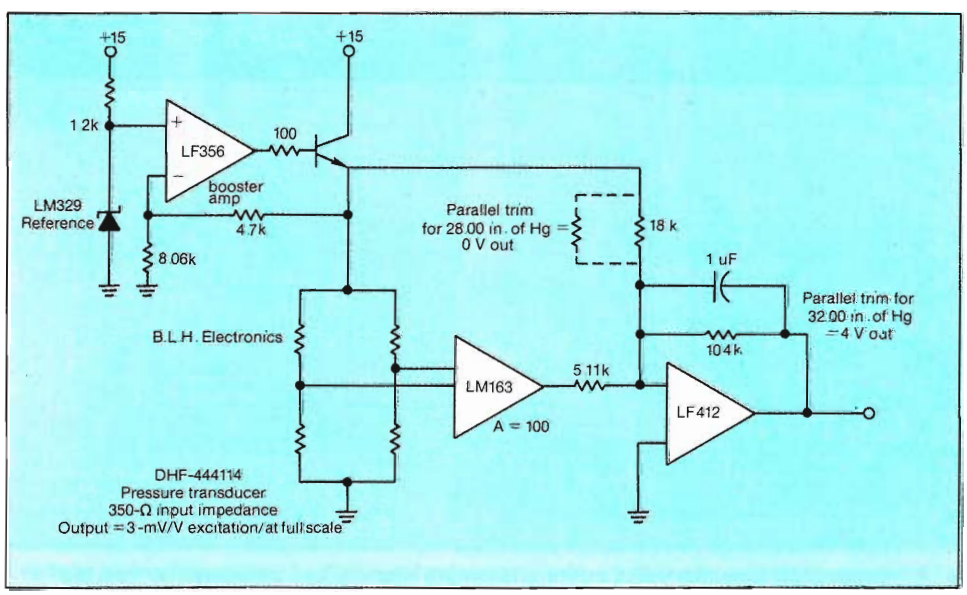
A general-purpose barometer

Barometric pressure can be very accurately measured using the circuit shown in Fig. 1. The drive voltage for the strain-gauge pressure transducer is derived from the zener reference and the booster amplifier. The 2N2219 transistor couples the 350-Ω impedance bridge of the transducer. The LM163 here extracts the differential signal from the bridge and amplifies it by 100. An LF412 operational amplifier receives the negative output of the LM163, and sums it with an offsetting positive reference current from the 2N2219's emitter.

The final amplification stage (at the LF412) should be adjusted so that the output of the LF412 will be zero for a barometric pressure of 28.00 inches of mercury. The resolution requirements of an analog-to-digital converter reading the output of the circuit are greatly reduced when 28.00-in. Hg is taken as the reference point (ambient pressure will generally remain above 28.00-in. Hg). As pressure increases, the output of the LF412 will rise accordingly. In this way, an integrating analog-to-digital converter with only 400-count resolution, preset to an output of 28.00-in. Hg ambient pressure, can be used to read pressure from 28.00-in. Hg to 32.00-in. Hg with a resolution of 0.01 in.

The offset adjustment will have to be changed to accommodate other pressure ranges. Most pressure transducers, however, are usually supplied with calibration charts showing precise offset and gain values. For the transducer specified, an accuracy of ±0.01-in. Hg may be expected over the ambient temperature range of 25° ±5.

Jim Williams, Applications Manager
National Semiconductor
2900 Semiconductor Dr., Santa Clara, CA 95051



1. A simple high-accuracy barometer can be made with a strain-gauge pressure sensor and the LM163. Offsetting the LF412 op-amp output for 28.00-in. mercury allows barometric pressure readings from 28.00-in. Hg to 32.00-in. Hg using an integrating a-d converter.

Figure 2 shows a circuit for conditioning the low-level signal output of thermocouple junctions, complete with cold-junction compensation. Because the current consumption of the cold-junction compensation circuit is on the order of 50 μA, the circuit can be battery-powered at a remote location some distance away from the LM163, and the battery life easily can extend up to five years.

In the circuit shown, an LM334 thermocouple generates a positive 0.33%/°C scaled current through resistor R_1 when the cold junction is close to it. Other adjustments can be accomplished with the TC-adjust potentiometer and the zero-adjust potentiometer. The first pot should be trimmed to the point where the voltage across R_1 equals the Kelvin temperature multiplied by the Seebeck coefficient of the particular thermocouple (see table). The zero-adjust pot should be trimmed until the voltage across R_2 equals the Seebeck coefficient multiplied by 273.2 (The table lists the necessary calibration data for various thermocouple types.)

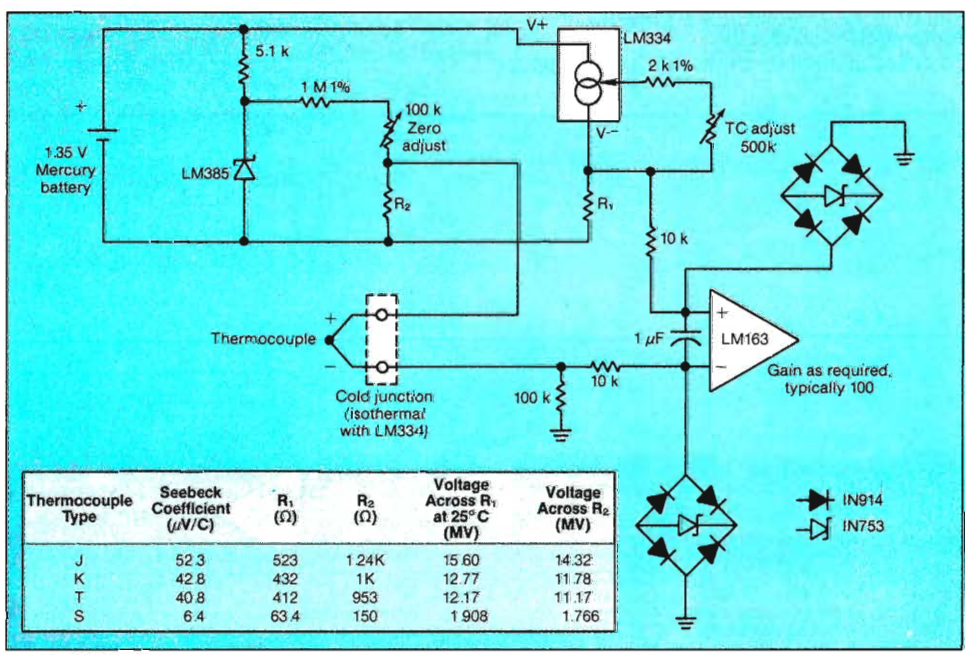
Gain for the LM163 may be set as desired. Because of its differential inputs, common-mode noise, which can frequently drown-out the microvolt-output of a thermocouple junction, is greatly reduced. The noise is reduced even more by cross-coupling the LM163 inputs with a 1-μF capacitor. The 10-kΩ resistors and the zener-diode bridges provide overvoltage protection for the LM163 under high-voltage fault conditions; the 10-kΩ resistor path allows the amplifier to receive a small bias current while keeping the thermocouple junction floating well above ground.

For precision temperature sensing and control applications, the LM163 can be used at high gain to read the output of a thermistor in a bridge configuration with some high-stability resistors. Figure 3 shows a servo-control circuit that can achieve sub-millidegree stability in a small oven. Operating at a gain of 1000, the LM163 amplifies the differential output of a bridge composed of high-stability wirewound resistors and a thermistor element.

The LM163 output is filtered by an adjustable RC time constant, which sets the frequency response of the controller. The output of the RC combination drives the LF356 for additional and adjustable gain. Following the LF356 output, an LM331 voltage-to-frequency converter is used to switch a heater element on or off through 2N2222A and LM395 drive transistors.

In operation, the thermistor element with a negative temperature coefficient will be at a high value when the circuit is first powered up. The LF356 will saturate in the positive direction, overdriving the LM331 input and biasing the 2N2222A off. This will keep the LM395 heater driver on until the oven comes to the set point established by the resistors in the bridge (in this example, 52.5°C). At that point, the circuit comes out of saturation, and the LM331 toggles at several kHz. The LM163, however, controls the state of the heater element (on or off) by controlling the frequency output of the LM331.

To optimize the circuit performance, the gain and

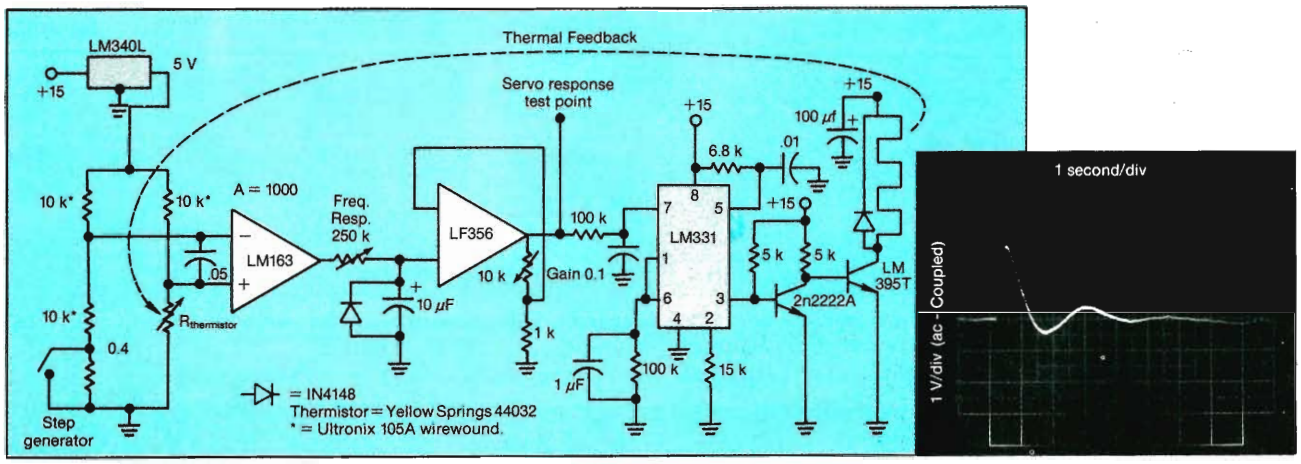


Thermocouple Type	Seebeck Coefficient (μV/C)	R_1 (Ω)	R_2 (Ω)	Voltage Across R_1 at 25°C (MV)	Voltage Across R_2 (MV)
J	52.3	523	1.24K	15.60	14.32
K	42.8	432	1K	12.77	11.78
T	40.8	412	953	12.17	11.17
S	6.4	63.4	150	1.908	1.766

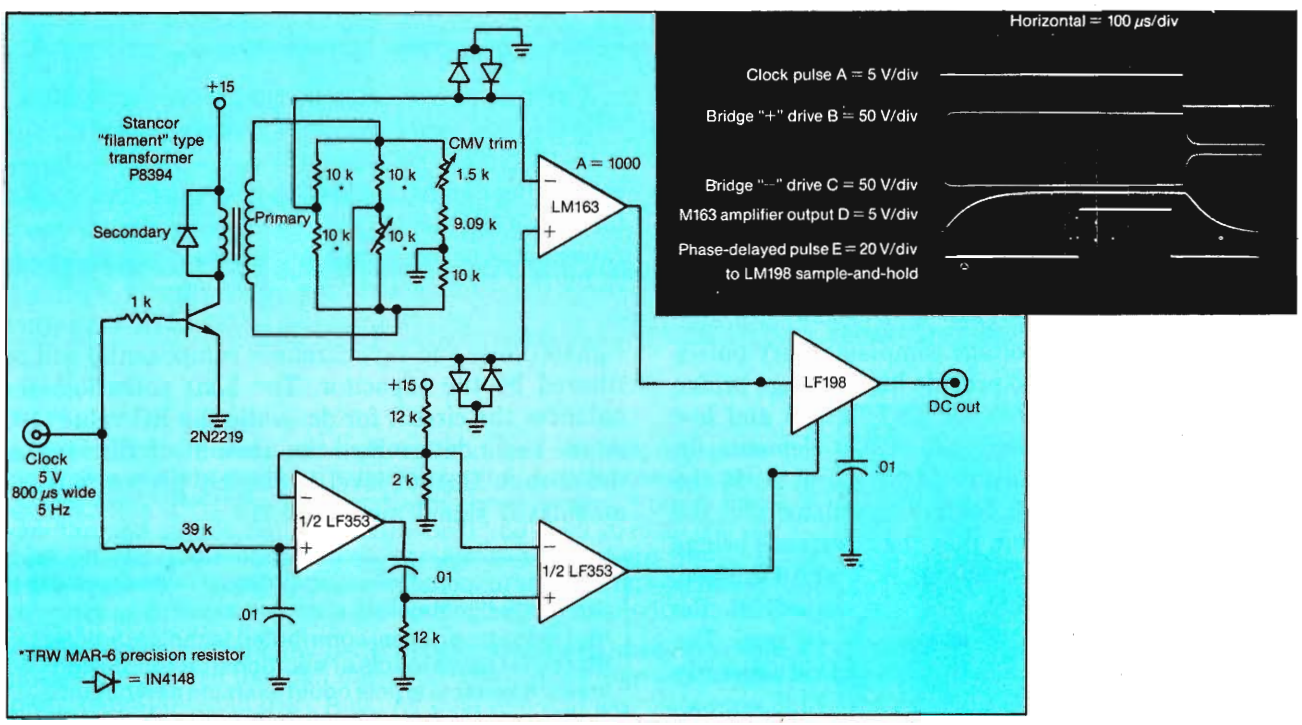
2. A thermocouple amplifier using a differential input amplifier can be located far from the thermocouple itself. The LM334 provides low-power cold-junction compensation that allows battery operation and long battery life. Resistors R_1 and R_2 should be chosen and TC and zero adjustments made for each thermocouple type (see table).

bandwidth of the circuit must be adjusted. A 0.4-Ω resistor switched into the sensing bridge should generate approximately 1-millidegree variation in the controller's set point, where the thermistor shifts about 380 Ω/°C at 10,000 Ω. The frequency-response and gain potentiometers are adjusted to obtain the fastest recovery from a simple step change at the input.

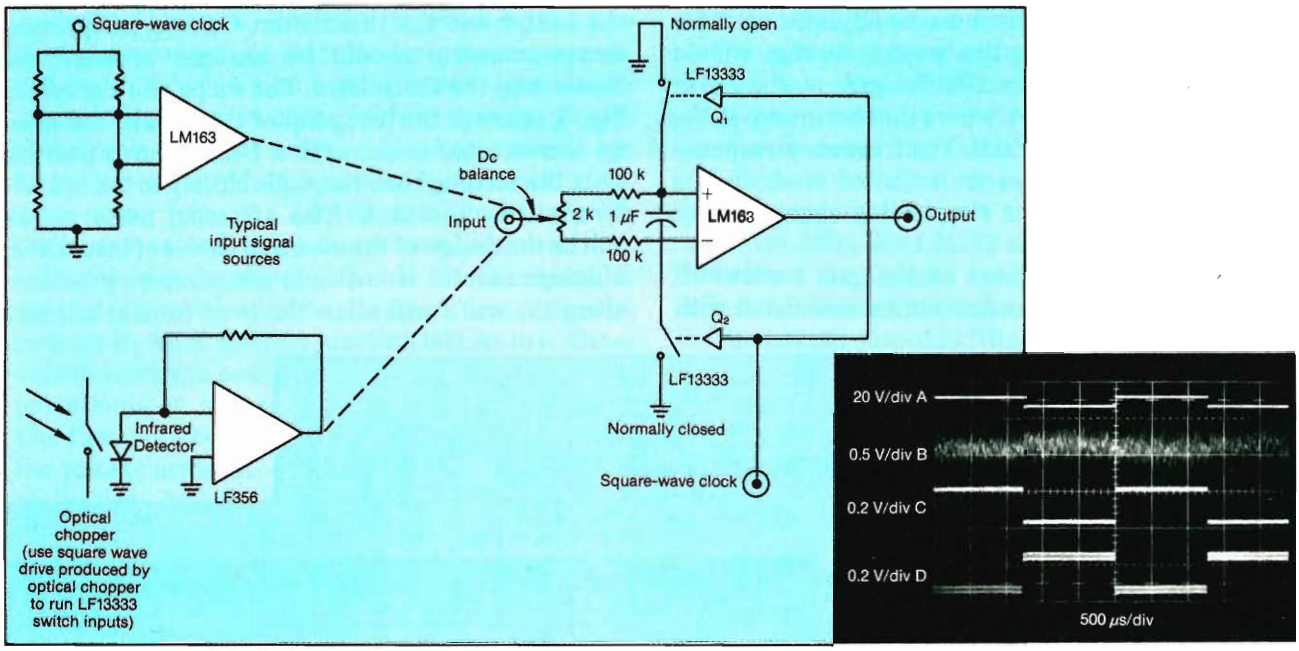
The ultimate limitations on the gain bandwidth of the circuit are the time constants associated with the heater and the thermistor. Consequently, tight thermalcoupling should be ensured between the heater and the thermistor. The scope photograph in Fig. 3, taken at the test point of the circuit, indicates an almost ideal response to a 1-millidegree positive step; the settling time responds closely to the heater-sensor time constant. Also affecting performance will be the design of the oven and choice of insulation, although careful attention to temperature gradients along the walls will allow the oven to hold setpoint



3. A temperature servo-control mechanism relies on a stable resistance bridge network with a thermistor element, a high-gain instrumentation amp, and a voltage-to-frequency converter to toggle a heating element. The servo responds in seconds to a millidegree change in temperature.



4. The resolution of a bridge-measuring system can be improved by pulsing the bridge with high voltage at low duty cycles. An 800-µs pulse (waveform A) will generate both 50 V (waveform B) and −50-V (waveform C) across the measuring bridge. The LM163 will produce a dc output (waveform D) with each pulse, which can be fed to the LF198 sample-and-hold. A pulse delayed through the LF353 will switch the LF198 into the hold mode as the pulse output of the LM163 appears.



5. The LM163, using a square-wave generator, can help extract a synchronous signal from a noisy transmission path. A square-wave pulse across the measuring bridge (waveform A) might be lost in noise (B) if not for the synchronous charging on each side of the 10 μF capacitor (C and D).

stability within 250 microdegrees.

Occasionally, very-high resolution measurement will require lower noise and drift combined with a wider dynamic range than an amplifier can provide. One way to increase the resolution is to increase the voltage input to the amplifier over a wider dynamic range, and thereby reduce the amplifier's proportional contribution to the input signal in terms of noise and drift. Unfortunately, transducer-bridge elements will dissipate only limited amounts of power and, therefore, will limit the extent to which the input voltage can be increased.

High-voltage bridge driving

One solution to this problem is to power the bridge with a series of high-voltage complementary pulses with a low duty cycle to provide high-voltage bridge outputs with zero common-mode voltage and low power dissipation through the bridge elements. In Fig. 4, the 5-Hz, 800-μs clock (waveform A, in the scope photo) biases the 2N2219 transistor and the P8394 transformer. From this, the resistance bridge receives ±50-V pulses (waveforms B and C). Here, the 1.5-kΩ potentiometer is used to adjust the common-mode voltage of the bridge to zero. The output of the LM163 (waveform D) will vary directly with the voltage across the bridge. An LF198 sample-and-hold amplifier changes the pulsed output of the LM163 into a dc signal, using a delayed pulse through the LF353 (waveform E).

When the output pulse of the LF353 is high, the LF198 samples the output of the LM163. When the pulse goes low, the LF198 goes into a hold mode with the sampled value. In this manner, the LF198 output is at dc and equal to the height of the LM163 pulses. The phase delay ensures that the LM163 has settled to its final value before sampling begins.

Simple synchronous demodulator

A simple and effective synchronous demodulator circuit can be used to extract a modulated signal from a 40-dB typical noise level (Fig. 5). Here, a square wave alternately applied to the plus and minus terminals of the LM163 and filtered by the 1-μF capacitor will represent an average signal value. Only the signals that are synchronous with the square wave will be amplified by the LM163; all other signals (noise and asynchronous components) will be filtered by the capacitor. The 2-kΩ potentiometer balances the circuit for dc, while the RC value (100 kΩ × 1 μF) determines the amount of filtering at the output. Output level is directly proportional to modulated signal amplitude.□

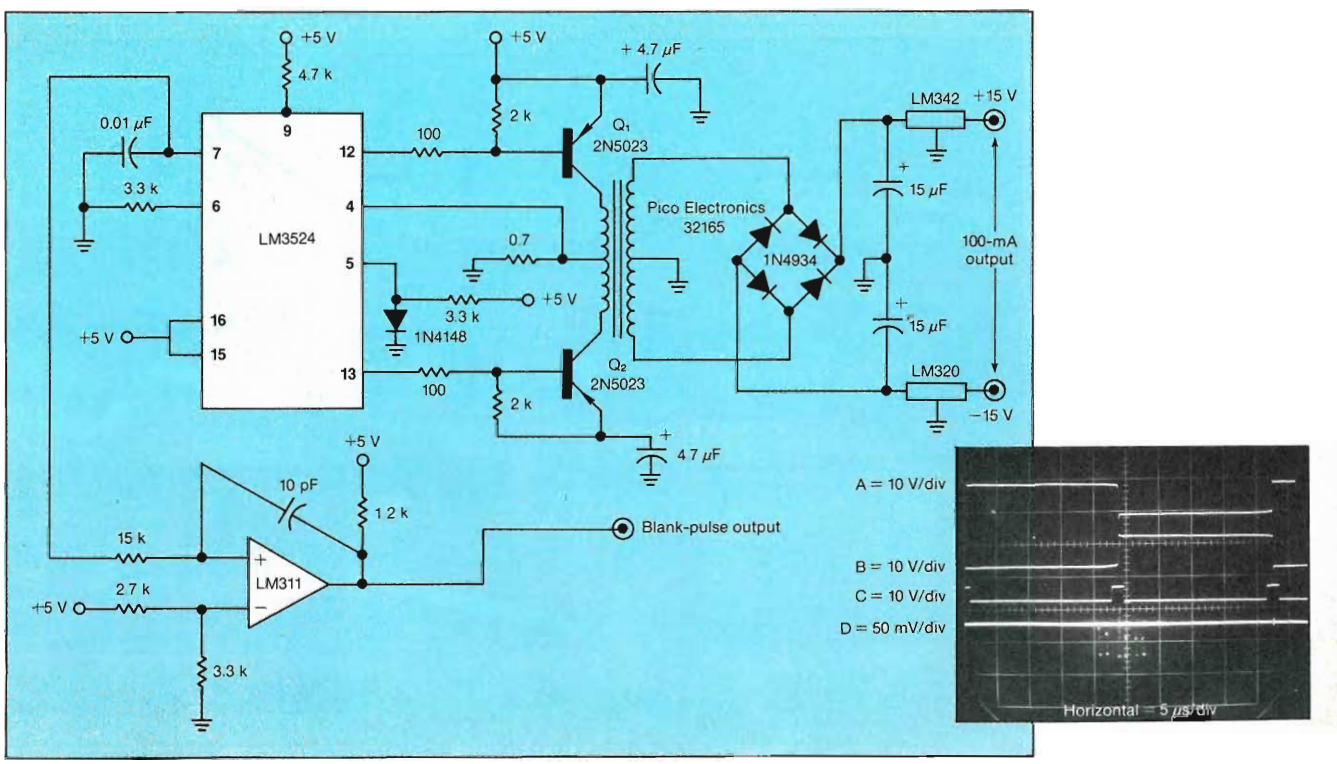
Design dc-dc converters to catch noise at the source

Systems-oriented dc-to-dc converter designs that take noise into consideration at the outset can substantially reduce, even eliminate, troublesome high-frequency switching spikes right at the source. In many applications, a high noise level is acceptable; but in data-acquisition and other systems working at 12-bit and higher resolutions, problems develop. If permitted to escape along the dc-dc converter's output line, noise spikes could have disastrous effects on critical circuit functions, such as analog-to-digital conversions.

For some system applications, changes in the dc-to-dc conversion process can reduce the noise to acceptable levels. For other system applications, noise spikes can be accurately predicted and denied an exit path from the dc-dc converter.

A conventional dc-dc converter contains the transistors, transformer primary, and associated components needed to form a self-driven oscillator. The output of the transformer secondary is rectified, filtered, and regulated. Typically, the transistors switch in a saturated mode at 20 kHz, providing high-efficiency square-wave drive to the transformer. The output filter capacitors are relatively small compared with those used in sine-wave-driven transformers, and overall losses are quite low. The high-speed, saturated switching of the transistors, however, generates high-frequency noise components. These manifest themselves as brief current spikes drawn from the converter's input supply and

Jim Williams, Applications Manager
National Semiconductor Corp.
2900 Semiconductor Dr., Santa Clara, CA 95051



1. In this two-pronged attack on noise, a nonoverlapping drive to the transistors eliminates simultaneous conduction to reduce input current spiking. A blanking-pulse output from the LM311 alerts a system of an imminent noise spike, so critical circuit functions can be delayed.

as high-speed spikes on the output lines.

Spikes occurring at each transition of the switching transistors are approximately 10 to 20 mV in amplitude. In addition, the transformer can radiate rf noise. Careful converter design—which means taking input filter construction, transformer selection, and package shielding into serious account—can reduce these problems.

In the examples that follow, the dc-dc converter is an active element in a larger system's operation, giving commands and accepting external control to provide a clean, noise-free source of power.

A blanking-pulse converter circuit shown in Fig. 1 warns of an imminent noise spike, giving its associated system time to delay critical a-d conversions or sample-and-hold operations. The circuit will supply 100 mA at ±15 V for a 5-V input.

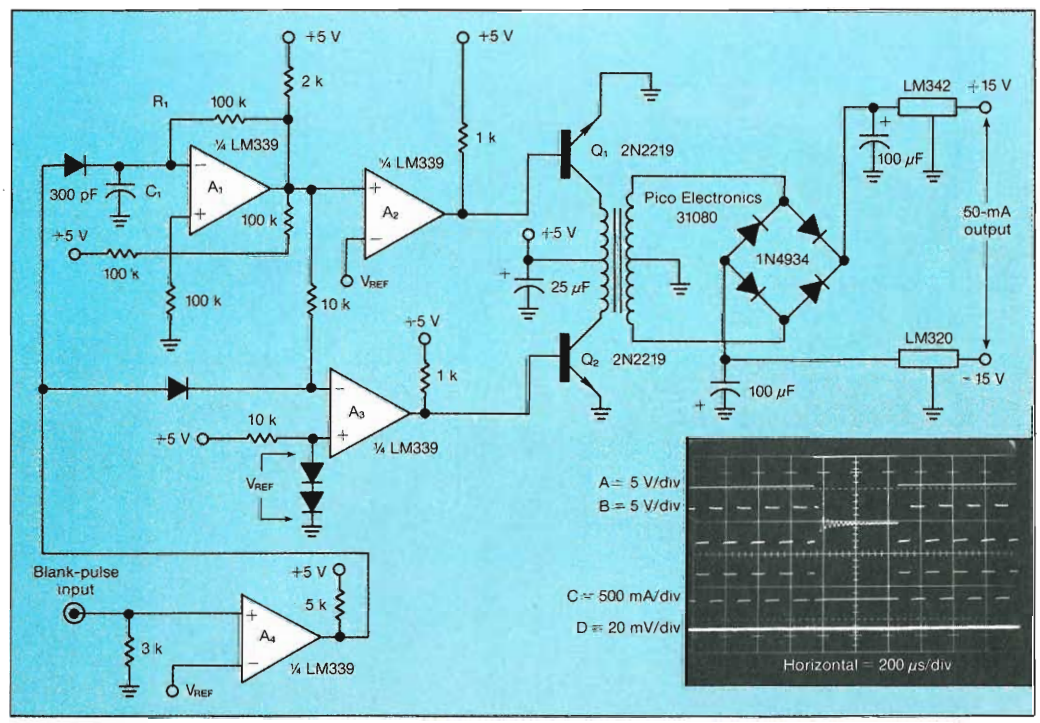
Noise, in this design, is attacked in two ways. The LM3524 chip's internal logic-switching regulator provides nonoverlapping drive to transistors Q_1 and Q_2, eliminating simultaneous conduction with its resultant input-current spiking and noise. The regulator operates in an open-loop fashion. The feedback connection (pin 9) is tied high, forcing the chip's outputs to a full duty cycle. The values of the components at pins 6 and 7 determine the switching frequency.

The LM3524's timing ramp biases the LM311 comparator, forcing it to generate a blanking pulse that "brackets" an output noise pulse at each switching transition. The pulse interrupts critical circuit operations during a noise spike. The 0.7-Ω resistor at pin 4 sets the short-circuit output to a maximum of 150 mA.

In Fig. 2, the "electronic tables" are turned. Here, the system warns the dc-dc converter of an impending critical operation and disables the converter's transformer for as long as required. The output regulators draw current from the 100-μF capacitors during the blanking period. The value of the capacitors depends on the output load and blanking duration, a limiting factor in this design.

In the externally strobed converter, A_1, which is part of the LM339 quad comparator, functions as a clock to drive comparators A_2 and A_3. These two drive transistors Q_1 and Q_2, which in turn provide power to the transformer.

When a critical system operation must occur, an external blank pulse (trace A) is applied to A_4, forcing that comparator's output high and shutting off all transformer drive. Transformer current (trace C)



2. A blanking-pulse input from the powered system turns off this converter during important analog-to-digital or sample-and-hold operations. Power for the system is drawn from 100-μF capacitors while the dc-dc converter awaits the end of the external blanking pulse.

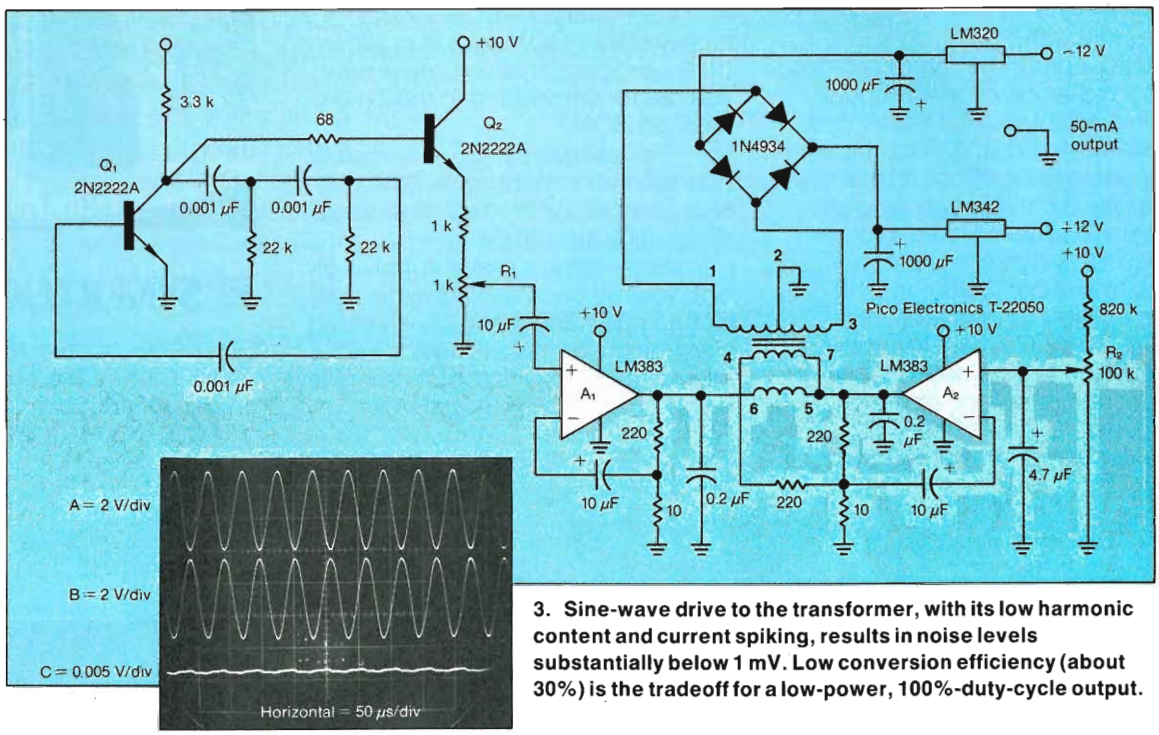
ceases and output noise (trace D) virtually disappears. Voltage ringing can be seen in trace B, Q_1's collector-voltage waveform.

If synchronization with a system is required, a system-derived 20-kHz square wave can be applied, through a 2-kΩ resistor, to A_1's negative input. Capacitor C_1 and the 100-kΩ feedback resistor, R_1, should be removed.

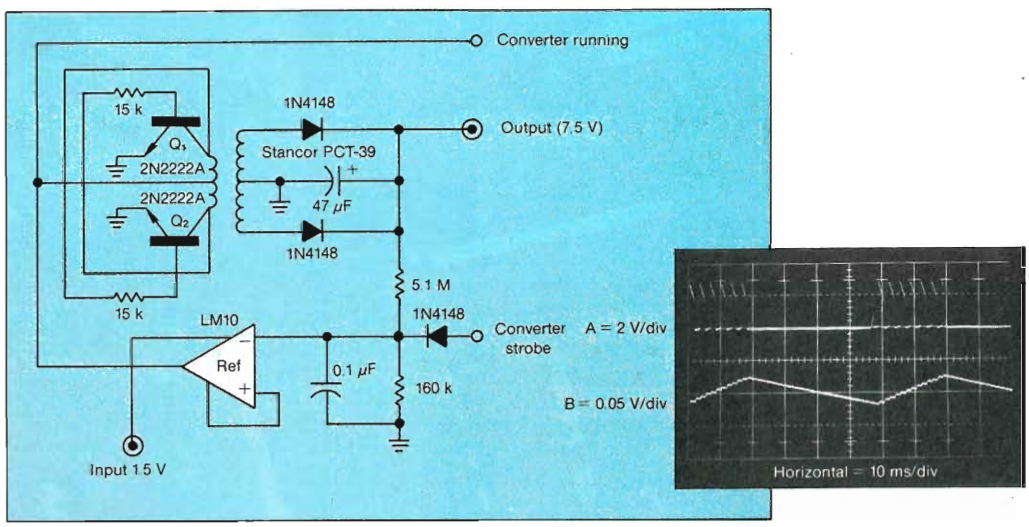
Less efficiency for 100% cycle

The off time of this circuit is limited by the storage capacity of the output filter capacitor. While this will present no problems for most systems, some will require a converter with both low-noise output and a 100% duty cycle.

Sacrificing the efficiency of saturated switch-mode operation in the sine-wave-driven converter shown in Fig. 3 yields a 100% duty-cycle circuit with an inherently low noise output. Since sine-wave drive contains little harmonic content and current spiking, output noise is well below 1 mV (trace C). Although the efficiency of this circuit degrades to as low as 30%, in low-power applications (50 mA, for example), this is often acceptable.



3. Sine-wave drive to the transformer, with its low harmonic content and current spiking, results in noise levels substantially below 1 mV. Low conversion efficiency (about 30%) is the tradeoff for a low-power, 100%-duty-cycle output.



4. An external strobe input allows this converter's oscillator to be interrupted when the lowest possible noise output is desired. A single D-size 1.5-V cell can provide a 7.5-V converter output suitable for microampere-level loads.

Transistor Q_1, a 20-kHz phase-shift oscillator, drives Q_2, an emitter follower. ICs A_1 and A_2 drive the transformer in complementary-bridge fashion (trace A and B). The high-current output of the amplifiers, in combination with paralleled transformer primaries, produce a high-power transformer drive signal. The transformer output is rectified, filtered, and regulated.

To adjust this circuit, the wiper arm of R_1 is grounded and R_2 is adjusted for minimum power-supply drain. The ground is then removed from R_1 and that potentiometer is adjusted for maximum output from A_1 and A_2 without clipping.

Whenever the lowest output noise is desired, the circuit in Fig. 4 can be externally strobed off. Suitable for very-low-power applications, this circuit provides a 7.5-V output from a single 1.5-V D cell. The converter will supply a 125-μA load current (typically 20 CMOS ICs) for three months.

How long Q_1 and Q_2 drive the transformer is directly related to the load resistance. The converter's output voltage is sensed by an LM10 voltage-reference IC that compares the converter's output with its own internal 200-mV reference. When the converter's output drops below 7.5 V, the LM10 output goes high, driving the oscillator formed by the transistors and the transformer.

The rectified output of the transformer charges a 47-μF capacitor. When the charge on the capacitor reaches a high-enough value, the LM10 output goes low and oscillation ceases. Trace A indicates Q_1's collector voltage while trace B shows the output voltage across the 47-μF capacitor. Each time the output voltage drops, the LM10 drives the oscillator, charging the capacitor and increasing the output voltage. For a low-noise output during critical system operations, a pulse applied to the LM10's negative input overrides normal converter operation.

The frequency of the regulating action is determined by the load's current requirements: Very low loading results in considerable off time; large loads may force almost constant oscillator action. Loop operating frequencies of 0.1 to 40 Hz are typical. In addition, the LM10 has an output to alert an associated system of converter operation.□

Circuit Design provides a forum for short (two to four magazine pages) contributed technical articles that cover new aspects of traditional circuit-design areas. A suitable article could examine new circuit techniques for motor controllers or filter design, or new applications for a device that has been commercially available for a year or less. ELECTRONIC DESIGN will pay a flat honorarium of $100 for published contributions.

Simple techniques fine-tune sample-hold performance

Although standard monolithic sample-and-hold circuits fill most requirements, special capabilities are frequently required to extend hold times, to speed acquisition times, and to reduce large-amplitude, high-speed spikes known as "hold steps." Readily available parts can enhance the performance of the basic sample-hold converter without prohibitive additional expense.

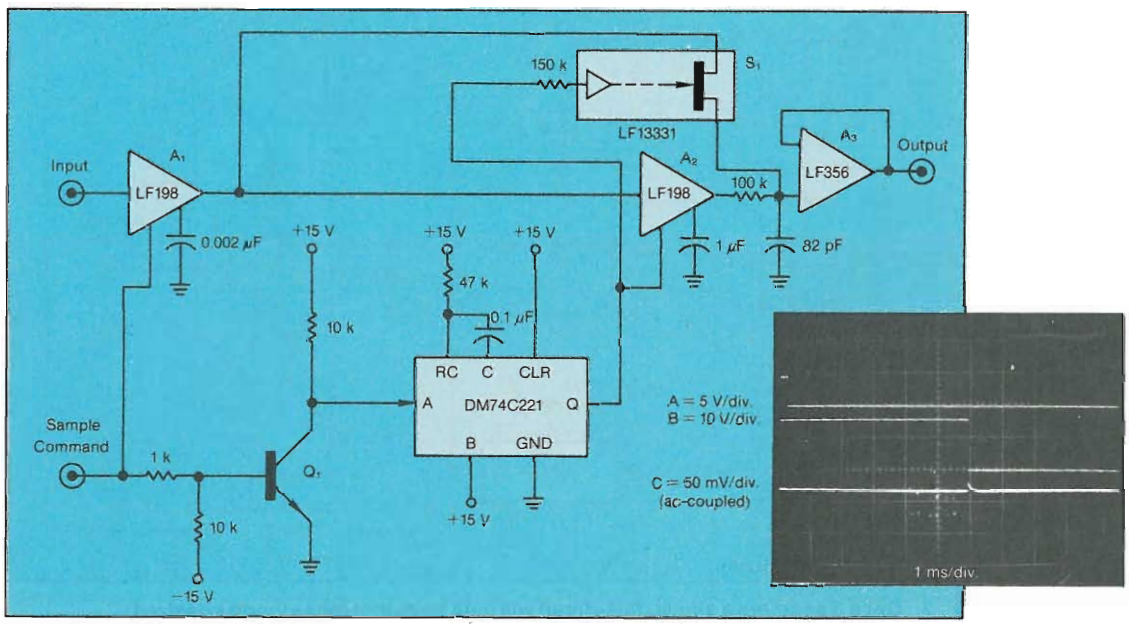
Hold time, for example, can be extended by "stacking" two sample-hold circuits in a chain (Fig. 1). In this circuit, rapid acquisition time is retained by use of a feed-forward path. When a sample command is applied to the circuit (trace A), sample-hold circuit A_1 acquires the input very rapidly because its 0.002-μF hold capacitor charges very quickly. The sample command also triggers the DM74C221 one-shot (trace B), which then turns on the FET switch, S_1. Thus, A_1's output is fed to the A_3 output buffer.

Jim Williams, Applications Manager
National Semiconductor Corp.
2900 Semiconductor Dr., Santa Clara, CA 95051

While the one-shot is high, A_2 acquires the value of A_1's output. When the one-shot drops low, S_1 opens, and disconnects A_1's output from A_3's input. At this point, A_2's output biases A_3's input. The circuit's output will not change from A_1's initial sampled value.

Trace C shows that a small glitch, caused by charge transfer through the FET, appears when S_1 opens. However, the steady-state output value does not change. This circuit will acquire a 10-V step in 10 μs to 0.01% with a droop rate of just 30 μV/s.

A circuit that extends the hold time to "infinity" with an acquisition time of just 10 μs is shown in Fig. 2. Once a signal has been acquired, this circuit will hold its output with no droop for as long as is desired. The divided-down output of sample-hold A_4 is fed directly to the circuit output via A_5 as soon as a sample command (trace A) is applied. The sample command also triggers the DM74123 one-shots. The first one-shot (trace B) biases the FET switch off during the time the one-shot is low. The second one-shot delivers a pulse to the ADC0801 a-d



1. Two sample-and-hold circuits, connected in a chain, extend hold time. Rapid acquisition time is maintained by using a feed-forward path.

converter, which then performs a conversion on A_4's output. D-a converter DAC-1020, combined with A_2 and A_3, converts the a-d converter's output back into a voltage. This analog-to-digital-to-analog conversion process requires about 100 μs.

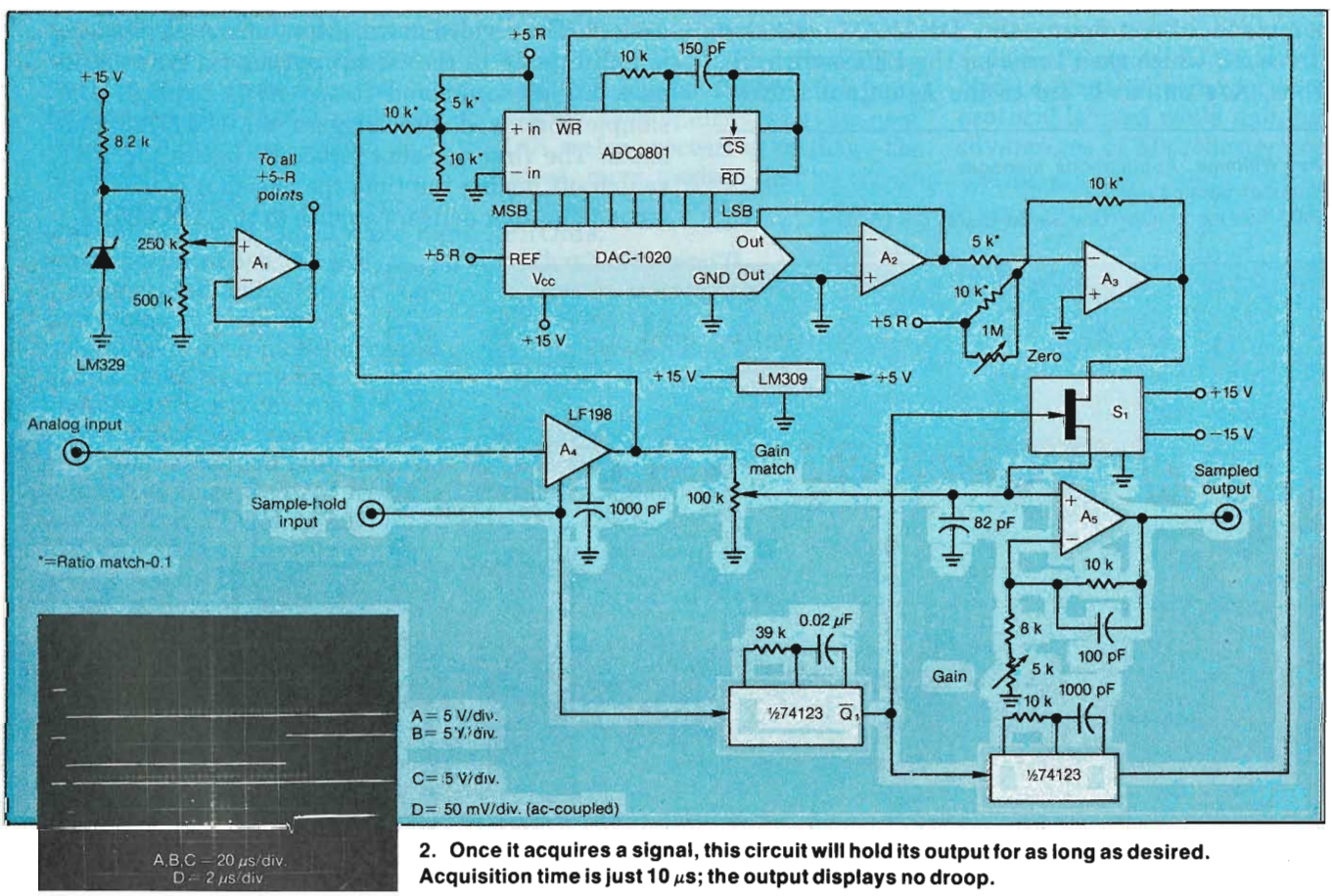
When the one-shot (trace B) times out, its output goes high and closes the FET switch. This action effectively connects A_3's output to A_5 while disconnecting A_4's output. The circuit output can thus remain at the dc level originally established by A_4's sampling action. Because the sampled value is stored digitally, no droop error can occur. The precision resistors used in the circuit provide offsetting capability for the unipolar a-d output so that a −10-V to +10-V input range can be accommodated.

To calibrate the circuit, 10 V is applied to the input and the sample-command input is driven by a pulse generator. The "gain match" potentiometer is adjusted for minimum "hop" at the circuit output when S_1 closes. Next, the input is grounded and the "zero" potentiometer is adjusted for 0 V. Finally, 10 V is applied to the input and the "gain" trim potentiometer is adjusted for a precise 10-V circuit output.

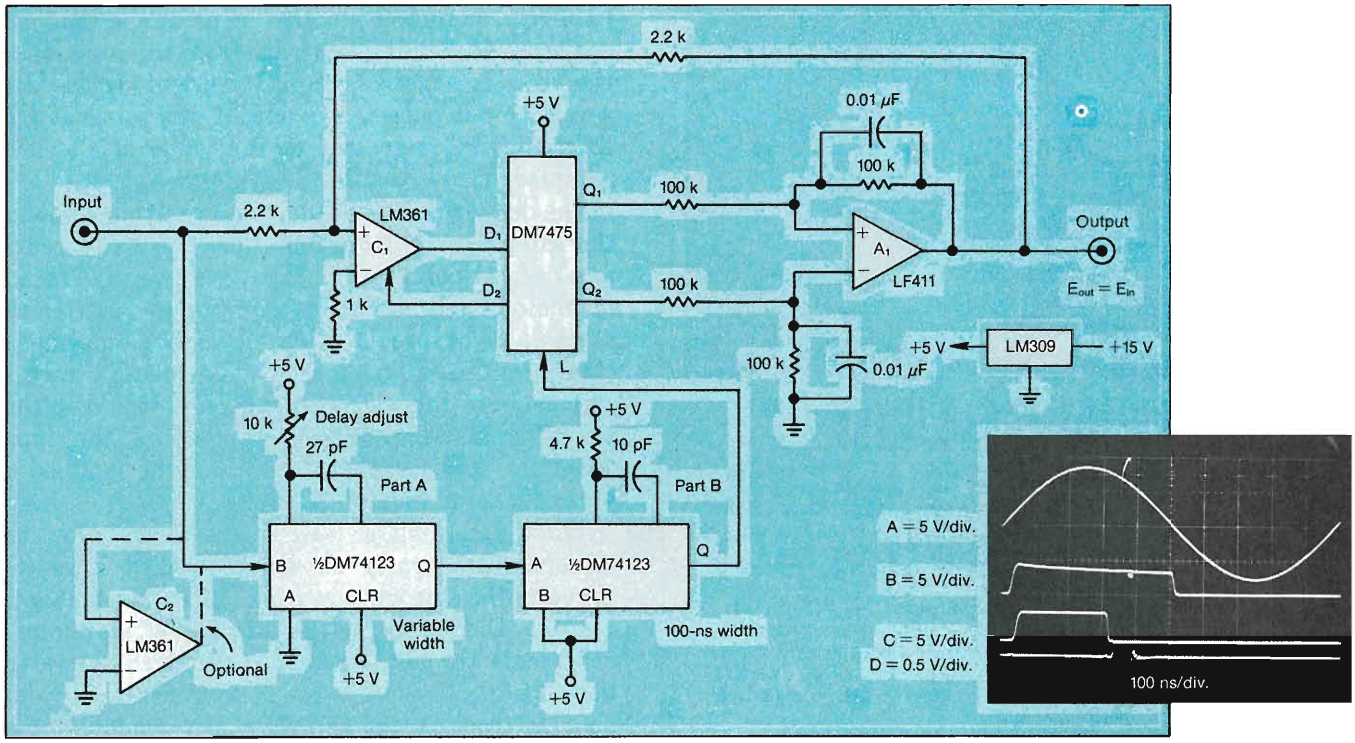
Once adjusted, this circuit will hold a sampled input to within the 8-bit quantization level of the a-d converter over a full range of +10 to −10 V. Trace D shows a small glitch caused by parasitic capacitance in the FET switch. The level shift is caused by quantization in the a-d conversion. An a-d converter with higher resolution could be used to minimize this effect.

Faster acquisition costs little

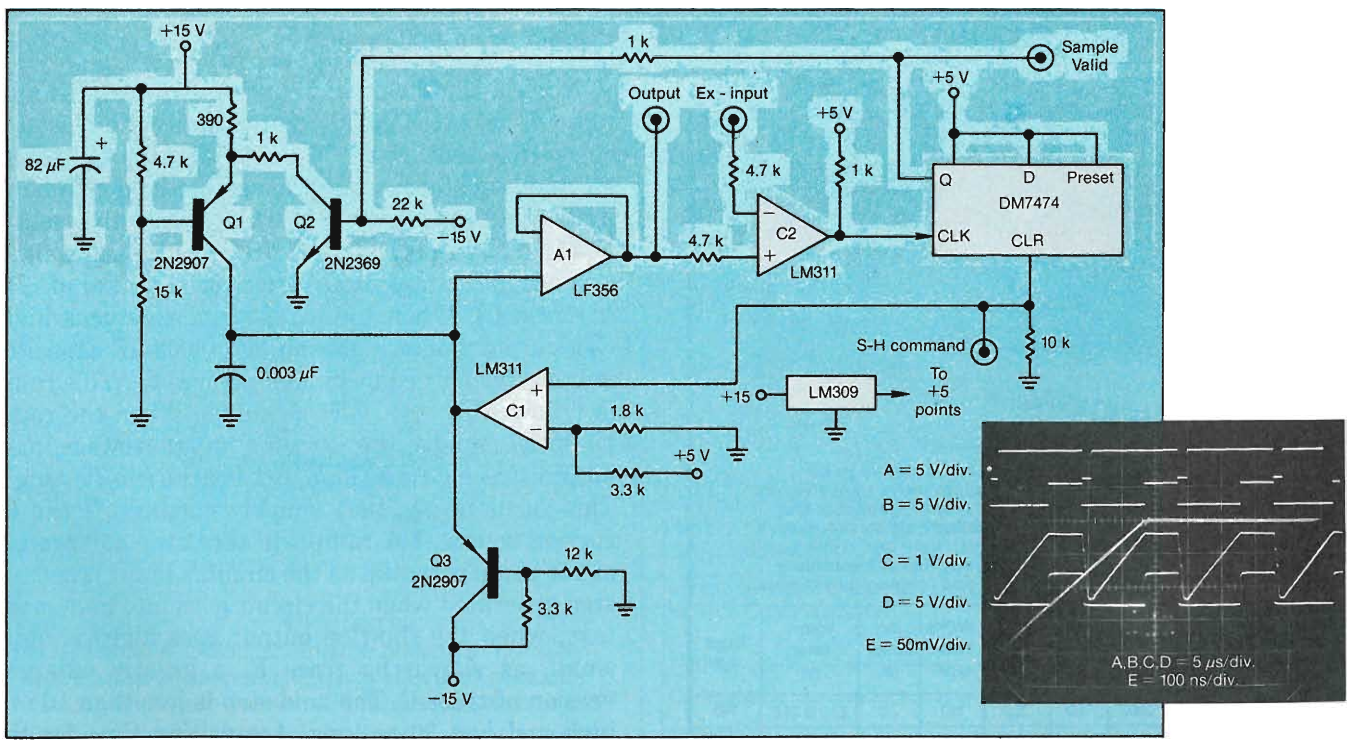
Conventional sample-hold circuits can be built for very fast acquisition times, but they will prove difficult and expensive to design. If the input waveform is repetitive, the simple and low-cost alternative shown in Fig. 3 can be used. Here, a very fast comparator and a digital latch are placed in front of a differential integrator. Feedback is used to close a loop around these elements. Each time an input pulse is applied, the DM7445 latch is opened for 100



2. Once it acquires a signal, this circuit will hold its output for as long as desired. Acquisition time is just 10 μs; the output displays no droop.



3. A very fast comparator and a digital latch combine to produce a sample-hold circuit with rapid acquisition times. The input waveform must be repetitive.



4. This circuit reduces a hold step to less than 10 mV high and 30 ns long.

ns. If the summing junction error at the LM361 is positive, A_1 will draw current from the junction. If the error is negative, the inverse will occur. After several input pulses, A_1's output will settle at a dc level that is equivalent to the value of the level sampled during the 100-ns window.

The delay time of one-shot A is variable, allowing the sample pulse from one-shot B to be placed at any desired point on the input waveform. Trace A in photo A represents the circuit input. After the variable delay provided by one-shot A, one-shot B generates the sample pulse represented by trace B. The delay in this circuit has been adjusted so that sampling occurs at the midpoint of the input waveform. However, any point may be sampled by correctly adjusting the delay.

When sampling a 1-MHz sine-wave input, the optional comparator shown in dashed lines (C_2) converts the sine wave into a TTL-compatible signal for the DM74123 one-shot. Trace A in photo B represents the sine-wave input while B shows the output of C_2. Trace C is the delay generated by one-shot A, trace D, the sample-width window output of one-shot B. This pulse can be positioned at any point on the high-speed sine wave, with the resultant voltage level appearing at A_1's output.

Holding down hold step

While a sample-hold circuit is switching sample to hold, hold step could occur; usually the reason is capacitive feedthrough in the FET switches. In Fig. 4, sampling starts when the sample-hold command input goes low (trace A). This action also sets a DM7474 flip-flop low (trace B). At the same time, C_1's output clamps at Q_3's emitter potential of -12 V (trace C). When the sample pulse returns high, C_1's output floats high and the 0.003-μF capacitor is linearly charged by current source Q_1. This ramp is followed by A_1, which feeds C_2. When the ramp potential equals the circuit's input voltage, C_2's output (trace D) goes high, setting the flip-flop high. This turns on Q_2, very quickly cutting off the Q_1 current source. The ramp will then stop and remain at the same potential as the circuit's input. The hold step generated when the circuit goes into hold mode (e.g., when the flip-flop output goes high) is quite small, as shown by trace E, a greatly enlarged version of trace C. The hold step is less than 10 mV high and just 30 ns long. Acquisition time for the circuit is 5 μs/V.□

One way to get around the limitations of an all-analog signal-conditioning system is to replace a portion of the analog components with digital elements. When this is done, the best of both worlds accrues.

μP-controlled measurements sharpen industrial processes

Combining analog feedback techniques with digital intelligence is an easy and effective way to overcome the limitations of wide-tolerance components and temperature-induced circuit drift, especially in industrial applications. Constructing a chain of high-precision analog-signal-conditioning components could prove not only expensive but also too delicate for the harsh environments. Moreover, a microprocessor's computing and decision-making power, when combined with an analog measuring system, can reduce uncertainties in tolerance and temperature by orders of magnitude.

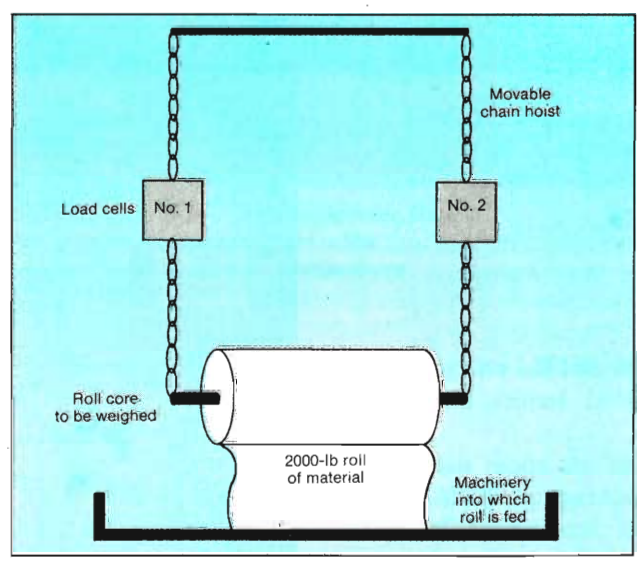
To see just how effective the analog-digital combination can be, consider a typical industrial application: performing highly precise, large-scale weight measurements to maximize the efficiency of an industrial process. Say that 2000-lb rolls of plastic sheeting material must be weighed before being fed into machinery that uses the plastic sheeting in a coating operation. Because this plastic is very expensive, as much of it as possible must be used before putting on a fresh roll.

However, if the plastic sheeting runs out before a new roll is spliced, the new roll must be rethreaded through the machinery, causing an expensive delay in production. Consequently, to detect small quantities of plastic remaining on a 2000-lb spool requires a high-resolution industrial scale, in this case one that reads to 0.2 lb, or 0.01% of full scale (Fig. 1). Other specifications include accuracy to 0.03% for a temperature range of 10 to 45°C (50 to 113°F). Field replacement of the load cell and a 20,000-count display are also required.

Unfortunately, standard components, such as load cells, often will not meet the specifications needed to achieve such tight resolution. Specifications for a typical high-quality, strain-gauge, load-cell transducer are gain slope of 3 mV/V excitation ±0.1%, excitation of 10 V, gain temperature coefficient of ±0.0008%/°F, and zero temperature coefficient of ±0.0015%/°F. From this information, it becomes apparent that the load cell's margin for error precludes meeting system requirements.

For example, 3 mV/V means that only 30 mV of full scale is available for a typical 10-V transducer excitation. Yet the scale's 0.01% resolution requirement means that only 3-μV error is permissible at the transducer output.

The gain-slope tolerance and temperature coefficients of the load cell, while small, also prevent meeting the required specifications. Complicating matters further, the same 0.1% gain slope tolerance between load cells suggests the need for manual recalibration whenever load cells are replaced.



1. Industrial settings often pose difficult measurement problems. To weigh a 2000-lb spool to within .01%, or 0.2 lb, standard components such as load cells often will not meet the needed specifications.

Jim Williams, Applications Manager
National Semiconductor Corp.
2900 Semiconductor Dr., Santa Clara, CA 95051

Even if these specifications are met, the need for an analog-to-digital converter precise enough to hold near-15-bit stability over the temperature adds to the designer's woes.

The key to achieving the desired performance is to realize that the system can be designed as an integrated function instead of a group of interconnected signal-conditioning blocks. Traditional approaches that rely on "brute force"—using high-stability amplifiers and data converters—cannot be successfully used here.

Figure 2 shows an effective solution. In this arrangement, an INS8070 microprocessor closes an analog loop around the two load cells, an LM163 instrumentation amplifier, and a discrete component a-d converter.

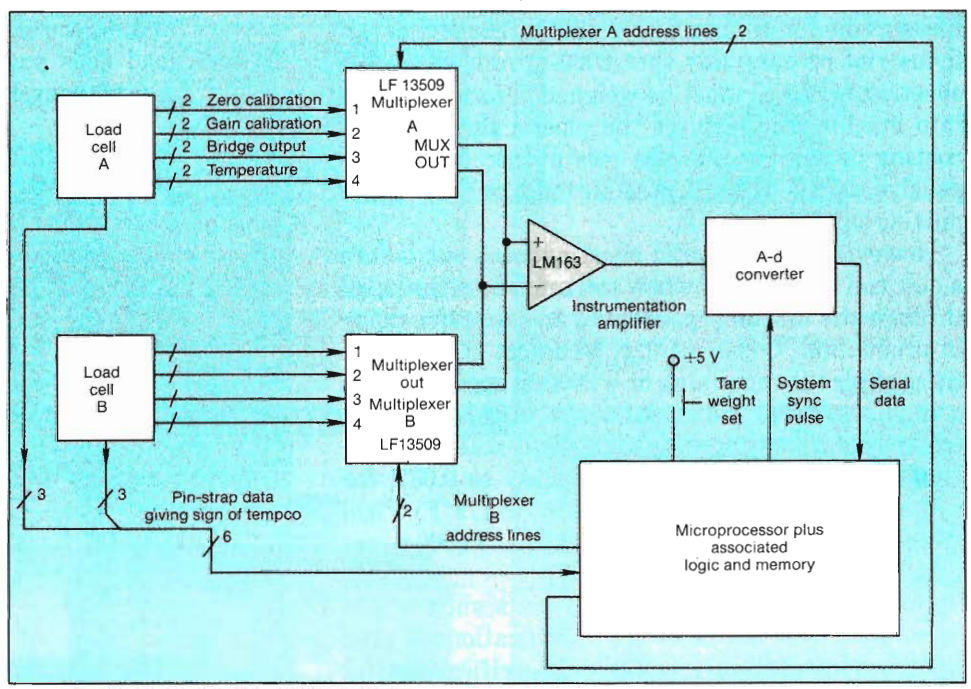
Four separate measurements are continuously performed on each load cell to determine its output and correct any errors. Corrections are made for zero offset, gain drift, and first-order temperature effects by multiplexing the error data to the a-d converter feeding the microprocessor. The final measurement is the uncorrected load-cell output voltage.

In addition to orchestrating the system operation and correcting the load-cell errors caused by temperature and gain-slope variations, the microprocessor automatically zeroes the scale and remembers the tare, or unloaded weight, and corrects full-scale errors. It controls the multiplexing between load cells and between individual measurements within a load cell. And it controls the a-d converter as well as averages the weight measurements to filter out the effects of system noise and overshoot.

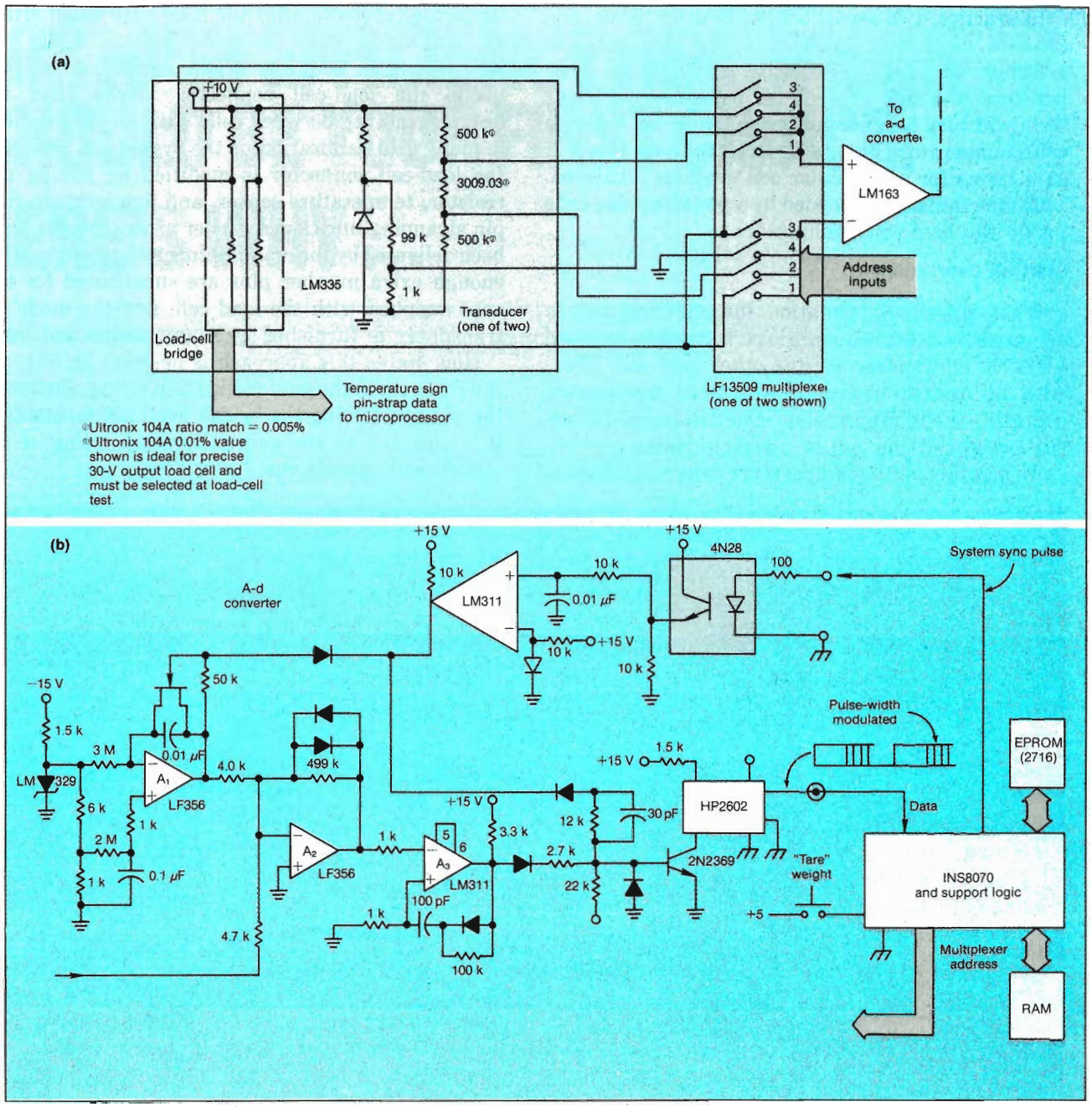
Setting cycle in motion

The measurement cycle starts when the microprocessor commands one of the two LF13509 differential input multiplexers to position 1. In this position, the LM163 instrumentation amplifier's inputs are connected to one side of the transducer bridge; this determines the electrical zero of the system at the bridge's common-mode output voltage. Actual physical zero information, e.g., the tare weight, is fed to the microprocessor when a pushbutton is pressed and there is no load in the chain hoist. This need only be carried out when the system is first turned on.

When zero is established for the load cell, the multiplexer switches to position 2. In this position, the LM163 inputs are connected across the middle resistor in a string of resistors (Fig. 3). The voltage across this resistor represents the precise full-scale output voltage of the load-cell transducer—in this case, 30 mV. Note that although the transducers are specified to be within 0.1% of any replacement unit, a more precise value of gain slope is furnished with each individual device. This information allows the system to determine the exact gain slope of each transducer, and automatically corrects for differences between them.



2. One solution to overcoming limited performance specifications is to add digital intelligence—in other words, computational and decision-making power—to the measuring function. Here, a microprocessor reads error-causing variables such as temperature, gain drift, and zero offset to help peak component performance.



3. In this weighing circuit, the transducer and associated circuitry feed data to an LF-13509 multiplexer, which drives an LM163 instrumentation amplifier (a). The transducer information is digitized and sent to the microprocessor, which orchestrates the sequence into a complete measurement cycle and remembers correction factors and averaging results (b).

The middle resistor in the string is located inside the load-cell connector. Thus, when a load cell is plugged into the system, the value of this resistor is read, giving immediate and precise gain slope compensation and so eliminating manual calibration. When this measurement is completed, the multiplexer switches to position 3. In this position, the output of one strain-gauge bridge (there are two in the system) is then connected to the LM163 instrumentation amplifier. This signal, which is the transducer output, is amplified by the LM163, converted by the a-d converter, and stored in the microprocessor memory.

The fourth multiplexer operation reads the temperature of the load from an LM335 temperature sensor located inside the load-cell transducer, and stores this value in memory. In this case, the relatively high level of the LM335 output is divided down by 100 using a resistor network so the LM163 does not saturate.

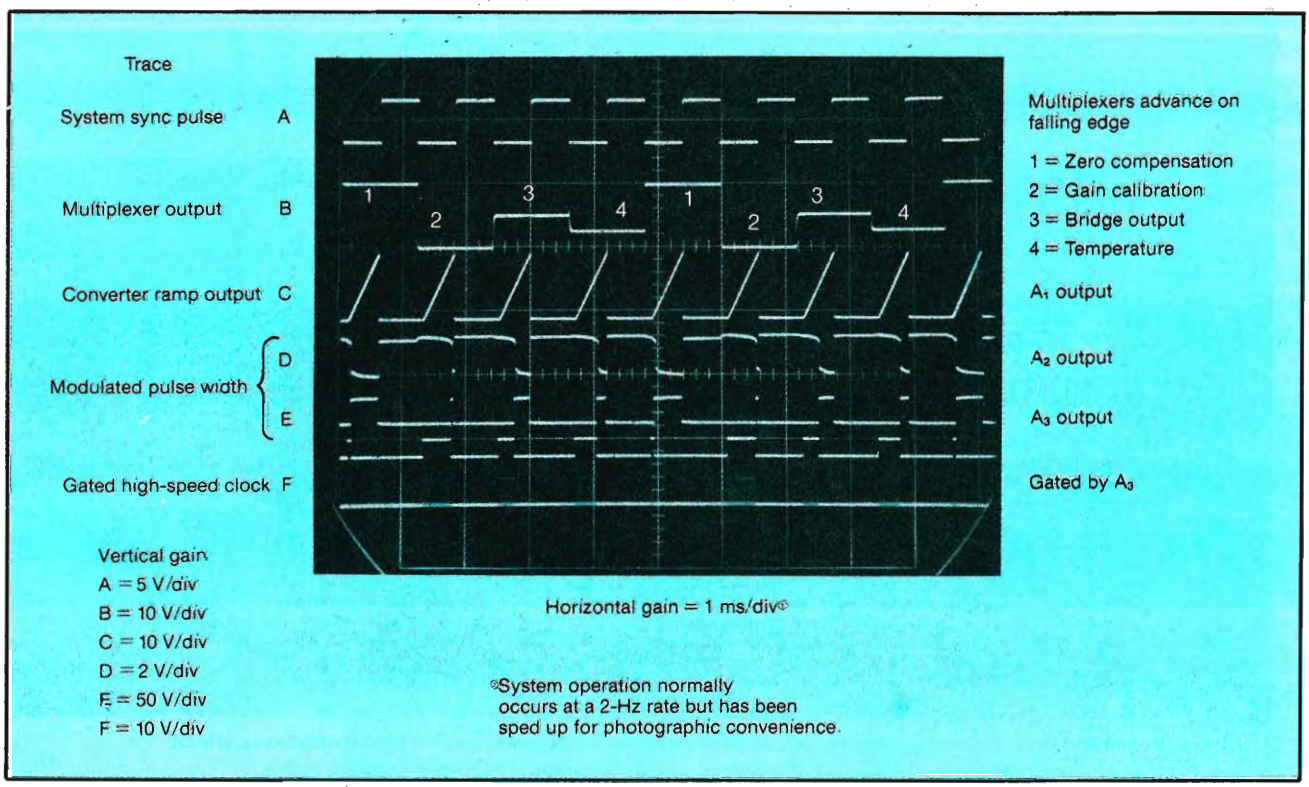
In practice, two separate temperature terms, one for zero and one for gain, affect the load cell, and although the LM335 provides absolute cell temperature, the sign of each temperature-coefficient term will vary between load cells. Thus, not only the cell's temperature but also the sign for both zero and gain terms for a particular cell must be furnished. This information is provided by a pin-strapping code inside the load cell's connector.

Start all over again

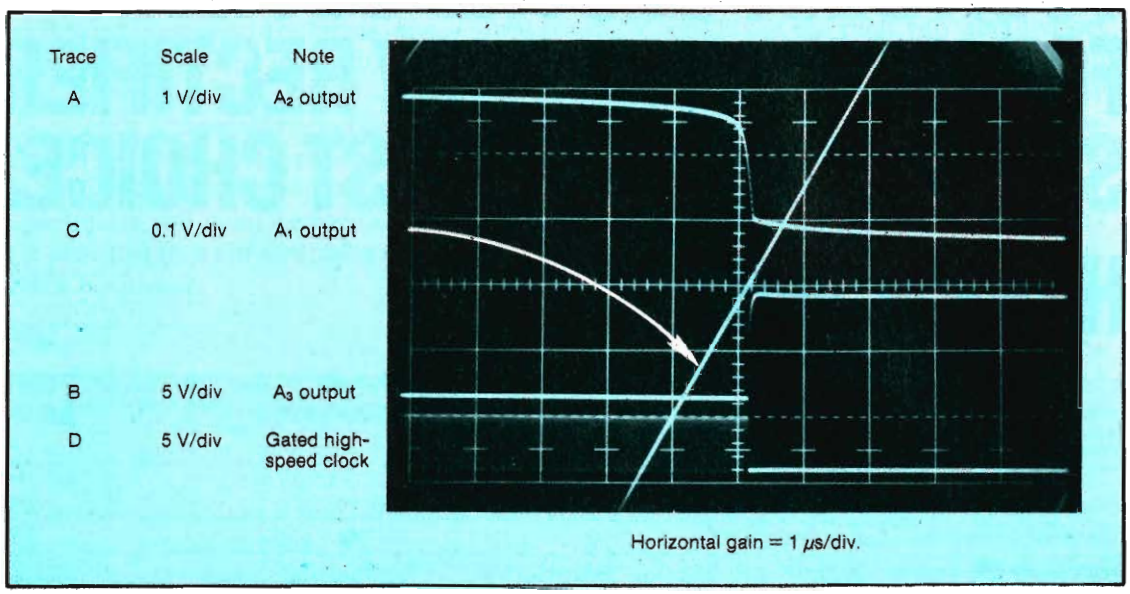
When all the information for one load cell is acquired, a similar sequence is performed by a second LF13509 multiplexer for the other load cell. Then, with all the information from both transducers collected, the microprocessor can determine the actual weight of the roll of plastic sheeting.

As mentioned, the temperature information gives first-order correction for the relatively small effect ambient temperature has on the load cell's gain and zero terms. In addition, a gain-correction resistor inside the load-cell connector allows field interchangeability between cells without the need for manual field calibration of the system. In practice, the load-cell connector is modified by adding the resistor, temperature sensor, and temperature-sign pin strapping mentioned earlier after the cells have been delivered by the manufacturer. Connectors with enough extra number pins are substituted for the ones supplied with the load cell, and the modified transducer is furnished as a unit to the end user.

How stable this approach is depends entirely on the resistors in the gain-calibration string. However, the voltage driving the bridge need not be stable—it is common to the gain-calibration string of resistors and cancels out.



4. Various probings along the circuit show the details of, among other signals, the system sync pulse, which advances the multiplexer address. Other crucial signals are the multiplexer output itself, the a-d-converter ramp and its pulse-width-modulated output, and the high-frequency clock gated by the PWM pulse.



5. When the ramp causes the output of comparator A_2 to switch, A_3 delivers a clean, noise-free transition, which disables the high-speed clock. Trace C shows the ramp greatly expanded, with the trip point occurring just after the ramp passes the center of the screen.

Low-pass filtering reduces electrical and mechanical noise and is achieved by displaying the average value of 10 to 20 measurement cycles. Note that zero and gain drifts in the LM163 instrumentaion amplifier and the a-d converter are continuously compensated for by the closed-loop action of the microprocessor. The sole requirement for these components is that they be linear and have noise limits within the specified measurement precision. This way the zero and gain drifts of all active components in the system are eliminated, which considerably simplifies the selection of these components and the system design as well.

The circuit details are shown in Fig. 3. For clarity only one load cell and its multiplexer are shown and details of the INS8070 microprocessor are omitted.

As described earlier, the LF13509 multiplexer feeds the LM163 instrumentation amplifier. The LM163's output drives the a-d converter section, which is composed of a ramp generator (A_1) and a precision comparator circuit (A_2 and A_3). The output of the a-d converter is pulse-width-modulated by the LM163's output and feeds the INS8070, which uses the pulse to gate a high-speed clock. The loop is completed by using the INS8070 to control the LF13509's address inputs.

Figure 4 illustrates how the system operates. Here, trace A is a synchronizing pulse generated by the INS8070. Trace B is the output of the LM163, which is connected to the multiplexer. Each time the synchronizing pulse goes low, the multiplexer advances to the next channel. The leftmost multiplexer state in trace B is the zero signal. The next state is the gain calibration, which is followed by the strain-gauge bridge output and then the temperature signal. The next four multiplexer states repeat this pattern for the other load cell.

Each time the multiplexer changes channels to read the next value, the LM163 output is compared with the ramp-generator output shown in trace C by the comparator formed by A_2 and A_3. Here, A_2 acts as a preamplifier for the A_3-based comparator, thus ensuring a low-noise trip point.

When the ramp voltage balances the current being pulled out of A_2's summing junction by the LM163, A_2 is no longer diode-bound and trips A_3. This is shown in trace D of Fig. 4. The rapid-slew, high-level signal from A_2 gives A_3's output a noise-free transition as shown in trace E of Fig. 4. This output is used to turn off a high-speed clock (trace F, Fig. 4), which was started at the beginning of the ramp.

Details of the comparator ramp and high-speed clock signals are shown in Fig. 5. These waveforms show that the number of high-speed clock pulses occurring for each multiplexer state varies with the LM163's output and hence each transducer variable. Because the ramp ishighly linear and the comparator is precise, a direct relationship exists between the number of high-speed clock pulses and the LM163 output. The final answer computed by the microprocessor is free of effects of drift in the a-d converter and the instrumentation amplifier.□

Design

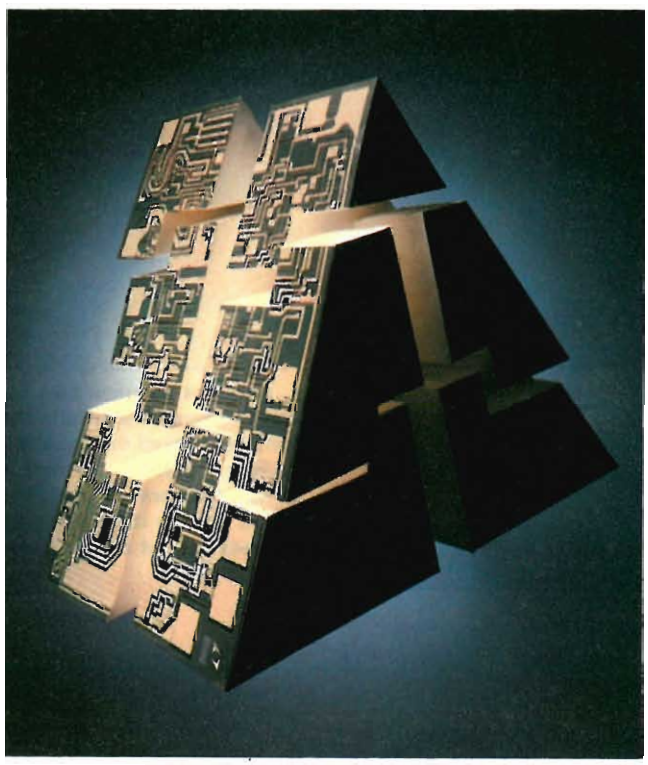
A new op amp stands ready to solve almost any data acquisition problem by blending the best input specifications of existing monolithic devices. It draws little power, too.

Precision op amp serves host of design needs

For a single op amp to be useful in a wide variety of applications, from buffer to integrator, it must have a combination of specifications that include low offset voltage, small changes in offset voltage with temperature, low bias current over its operating temperature range, and low noise—the lower, the better. If it uses little power, too, that is an added bonus.

Of course, general-purpose monolithic op amps have been around for years—for example, the ubiquitous 741. More recently, BIFET versions were added. But that contradiction in terms—the op amp that is general-purpose and at the same time precision—has only now made its appearance.

Devices have been available that excel in offset voltage and noise specifications, but then their bias currents are in nanoamperes, not picoamperes, and like the 741 they use milliamperes, not microamperes, of supply current. BIFET versions have very low bias currents but only at room temperature: the current climbs exponentially with temperature. On the other hand, though Darlington-input devices have bias currents in the low picoamperes over a wide temperature range and use low supply current, they are notoriously noisy. None seem to offer all the desirable attributes in one device.



George Erdi, Engineering Staff Vice President
Jim Williams, Staff Scientist
Linear Technology Inc.
1630 McCarthy Blvd.,
Milpitas, Calif. 95035

The new LT1008/LT1012, however, does—it is a true universal precision op amp. The offset voltage is a mere 25 μV, offset voltage change with temperature is 0.2 μV/°C (as good as the chopper-stabilized op amp class), and bias current is less than 80 pA from −55° to +125°C. As for noise, it is less than 500 nV peak to peak from 0.1 to 10 Hz. Not only that, but the circuit operates on less than 380 μA.

The 1008 and the 1012 differ only in frequency compensation. The internal frequency compensation of the 1012 provides a unity-gain bandwidth of 800 kHz, whereas the 1008 has a gain-bandwidth product of 5 MHz at a gain of 10. Moreover, the Bode plot (frequency response curve) of the 1008 is shaped with but a single external capacitor.

At first glance the major use for the 1008/1012 is in applications that require all its notable features—for example, a very simple buffer for a saturated standard cell. These cells cannot tolerate continuous current loading and the 1012's 30-pA bias current at room temperature causes an error of less than 1 ppm/year. Further, its superior noise and offset voltage characteristics are consis-

tent with such accuracy. Moreover, the 380-μA supply current drain provides long life when the op amps are used in a portable instrument.

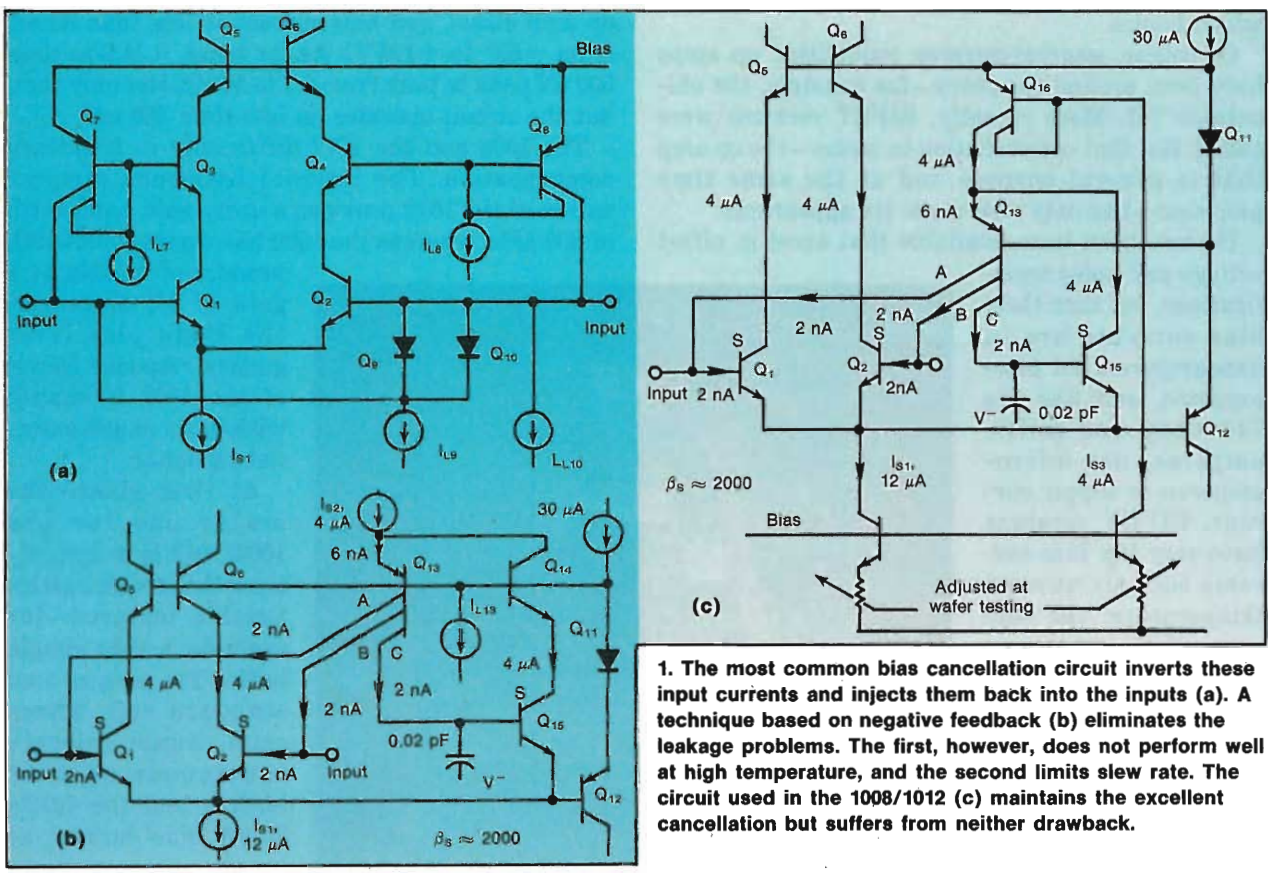
A similar application needing this op amp's combination of capabilities is a buffer for a five-decade Kelvin-Varley divider. When connected as a unity gain follower, the 1008 provides an error of less than 1 ppm. Other precision circuits needing such performance include integrators, current-to-voltage converters where noise gain is substituted for large feedback resistors, and instrumentation amplifiers with very high-input-impedance.

However, notwithstanding these special applications, the major advantage of the 1008/1012 may be in easing component stocking and error analysis for system designers. It is now no longer necessary to stock several different devices for precision applications; one for low offset and drift, one for low bias current or noise, and one for low power dissipation. The universality of the 1008/1012 permits its use for all but the most demanding, unusual, or high-speed analog signal-processing system. The difficult and time-consuming error analysis procedure for precision design and the ultimate compromises can be eliminated for most requirements.

The input offset voltage gains its microvolt levels by a zener-zapped trimming scheme at wafer sorting. Owing to a completly balanced input circuit, common-mode and power supply rejection are extremely high. The output is capable of delivering 5 mA of load current even with high voltage gain, although the total supply current is still only 380 μA (an accomplishment in itself).

Low bias current—how?

Picoampere bias currents are achieved without sacrificing noise and drift by using a unique scheme to cancel bias current. Bias current cancellation circuits have been used in the past (Fig. 1a). These circuits usually involve monitoring the input current (Q_3, Q_4), inverting it with pnp current mirrors (Q_7, Q_8), and injecting this current back into the inputs. These schemes work well at nanoampere levels. However, leakage from the pnp bases to the



1. The most common bias cancellation circuit inverts these input currents and injects them back into the inputs (a). A technique based on negative feedback (b) eliminates the leakage problems. The first, however, does not perform well at high temperature, and the second limits slew rate. The circuit used in the 1008/1012 (c) maintains the excellent cancellation but suffers from neither drawback.

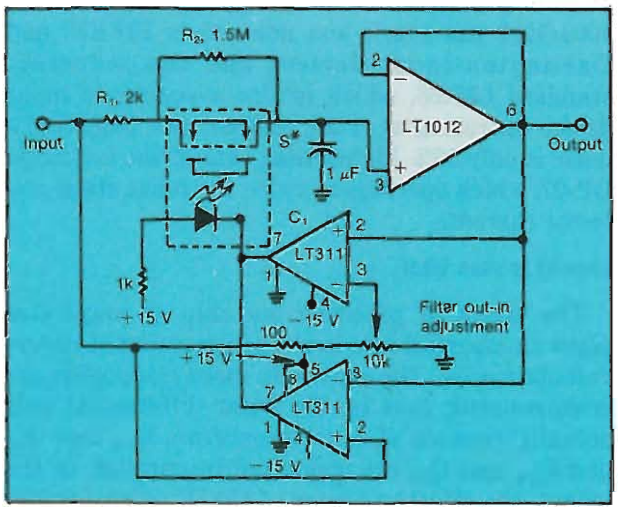
substrate (indicated by current sources I_{L7} and I_{L8}) can reach tens of nanoamperes at 125°C. An attempt can be made to cancel I_{L7} and I_{L8} using leakage from diodes I_{L9} and I_{L10}, but cancellation to picoampere levels is almost impossible.

These problems can be resolved by a different circuit (Fig. 1b). Q_1, Q_2, and Q_{15} are identical supergain transistors operating a 4 μA each. Through the feedback loop of Q_{13}, Q_{14}, and Q_{15}, the collector current of Q_{13A} and Q_{13B} will be an exact mirror of the base current of Q_{15}. The leakage from the base of Q_{13} (I_{L13}) has been removed from the bias-current cancellation path.

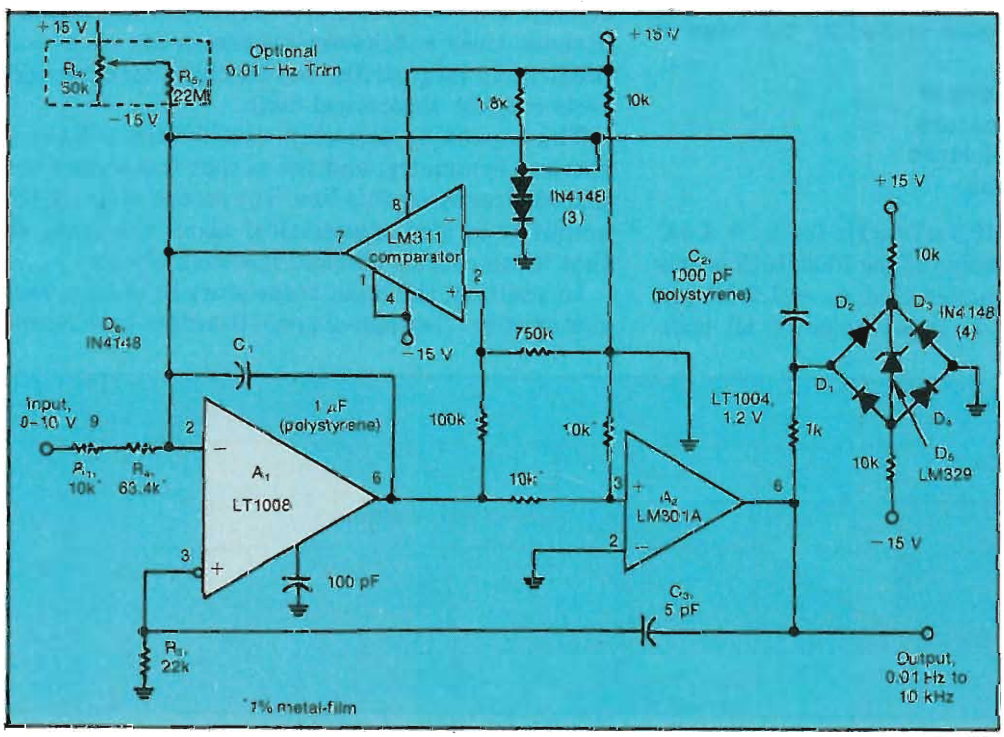
This circuit, however, suffers from a subtle problem while the inputs are slewing in the negative direction. The metal lead connecting the collector of Q_{13C} to the base of Q_{15} has to cross the isolation area between the two transistors. The capacitance of this lead to the negative supply is approximately 0.02 pF. This seemingly negligible capacitance is discharged by the 2-nA base current of Q_{15} (assuming a current gain of 2000). As the input slews negatively, the emitter of Q_{15} can move fast, but its base cannot. Consequently, most of the 12-μA I_{S1} current will be gathered by Q_{15}, significantly reducing the current available for the input transistors Q_1 and Q_2. These slewing problems distort ac waveforms to an unacceptable level.

The circuit in the 1008/1012 (Fig. 1c) eliminates the problem while maintaining the excellent bias cancellation features of the preceding approach. The Q_{15} collector current cannot increase; during negative slewing, Q_{15} will saturate, and the increased base current will rapidly discharge the 0.02-pF capacitor.

This cancellation scheme typically reduces the input bias current from 2000 to 130 pA. A fourfold reduction in the bias current (I_B) is achieved by



2. The low offset voltage and low bias current of the 1012 make possible a low-pass filter that grabs a new signal fast but still filters low-frequency noise when it appears later. The optically coupled FET, S, and the pair of comparators switch R_2 in and out to change the filter time constants.



3. The low bias current and low offset voltage of the 1008 join to build a high-performance integrator that extends the operating range of a charge-pump V-F converter.

zener-zap adjustment of current sources I_{S1} and I_{S3} at wafer testing. Obviously, in order for such an adjustment to be meaningful, the input bias current has to be measured to picoampere accuracies in a light- and noise-free environment. (Because the bias currents of BIFETs double every 10°C, compensation schemes such as this, even when used, do not provide the necessary low input currents at high temperature for these devices.)

In this zener-zap scheme, the range of adjustment is a function of the gain of the supergain transistor. Thus, when most needed—when the current gain of Q_1, Q_2, and Q_{15} is lower than nominal—the input bias current is likely to be high and the I_B adjustment range is large. Conversely, for higher-than-nominal supergain transistors, more fine tuning is possible with a reduced I_B trim range.

Lastly, the scheme prevents leakage over the −55° to +125°C by optimizing input transistor geometries and collector-base voltages.

Down with noise

The voltage noise of the 1008/1012 approaches the theoretical value for an input-stage operating current of 4 μA. The voltage noise density (e_n) of a differential pair of transistors is given by:

$$e_n = \{8kT[(kT/2qI_c)+r_b]\}^{1/2}$$

where:

r_b = the intrinsic base resistance underneath the emitter in series with the resistance from the base contact to the edge of the emitter.
k = Boltzmann's constant
T = absolute temperature
q = charge on the electron
I_C = collector current

When $r_b = 0$, $e_n = 10.5\ nV/\sqrt{Hz}$ for $I_C = 4\ \mu A$. The observed 1000-Hz noise of the 1008/1012 is only 14.0 $nV/\sqrt{Hz}$. That implies that $r_b = 1.5\ k\Omega$ and that the contribution to input noise of all transistors and resistors other than the input differential pair is about 10%. The sheet resistance under the emitter of a supergain transistor is approximately 60 kΩ/sq at betas of 2000. The supergain input transistor structure and geometry reduce r_b to 1/40 of a square, minimizing the base resistance component of voltage noise.

The noise at 10 Hz is only 17 $nV/\sqrt{Hz}$, indicating a low 1/f corner of 2.5 Hz, and from 0.1 to 10 Hz the peak-to-peak noise is only 500 nV. In fact, the 1008/1012 has much less noise than BIFET- and Darlington-input devices and the industry-standard LM108, which is also a supergain input device operating at 4 μA; indeed, the 1008/1012's noise is only 50% higher than that of the low-noise OP-07, which operates at twice the input stage collector current.

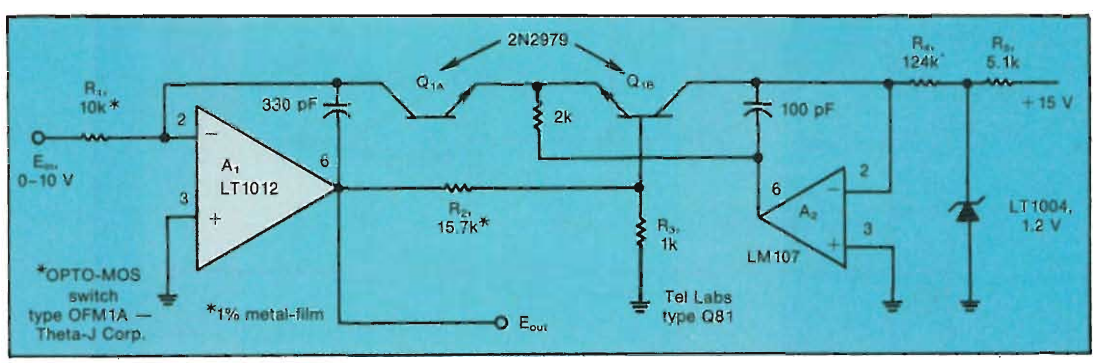
Layout is also vital

The layout of precision one-chip op amps also plays an essential role in the achievement of microvolt accuracies. The supergain input transistors are cross-coupled; that is, the input differential pair actually consists of four transistors. Q_{1A} and Q_{1B} and Q_{2A} and Q_{2B} are connected in parallel. In the layout, the effective center of the Q_1 pair coincides with the center of Q_2. This layout completely cancels thermal signals produced by the heat-generating output transistors.

Further, this cross-coupling decreases the effects of any gradients induced during processing or assembly. This is particularly important in low-drift designs, since nontheoretical errors can cause unpredictably large drifts, but on-chip trimming corrects only for theoretical drift.

The layout of the chip establishes a line of thermal symmetry, and the output transistors are placed directly on this line. The second stage of the amplifier is also symmetrical about this axis, so that it too cancels thermal feedback effects.

In addition, the input transistors have long, narrow emitters (lozenge-shaped) to reduce base resist-



4. In a typical logarithmic amplifier circuit the input characteristics of the 1012 produce over four decades of 99% conformity voltage logging, without offset trimming.

ance and therefore noise. Moreover, the input bias current cancellation circuitry (section 5) features a supergain transistor with emitter geometry identical to that of the input devices; consequently, current density and noise are the same for all five devices at the input.

A special effort was also made in the design of the multiple-collector pnp transistor (Q_{13}) used to supply base current to the input transistors. This transistor must operate properly with collector currents in the low nanoampere range—even at 125°C. Furthermore, these nanoampere currents must match in each segment of the transistor to within a few percent of each other.

Even though only three outputs are needed, a four-collector pnp device (with one collector current discarded) was used. Four equal collectors are easier to match on modern CAD equipment that generates chip geometries in only the X and Y coordinates. The area of each collector is as small as possible to reduce high-temperature leakage to a minimum. Finally, an extended subcollector, or buried layer, is used under the pnp transistor to hold down as much as possible the normal effect of shifts in the subcollector.

The bias current adjustment at wafer testing is achieved with the two zener-zap pads, and input offset voltage is permanently trimmed with the

The LT1008 vs its cohorts

The LT1008/1012 was designed to combine the best input and power characteristics of available op amps. The table compares the LT1008C with other precision op amps in the same price range. The highlighted areas give the salient specifications of the individual devices that were generally matched or bettered in the 1008/1012.

The OP-07C is the industry-standard precision bipolar op amp, the LF411AC is the BIFET representative, the LM11C is a supergain Darlington-input device, and the industry-standard LM308A was the first IC op amp to use a supergain input stage.

The offset voltage and drift of the LT1008 is slightly better than that of the OP-07, but the others trail by a wide margin. As for bias currents, those of the LT1008 and the LM11 are the lowest at 100 pA. However, the offset current of the LM11 is significantly lower, because bias current cancellation, which improves the bias current, does not appreciably reduce the offset current (the difference between bias currents at the two inputs). The OP-07 lags the field by more than an order of magnitude.

It should be noted that the bias and offset currents are compared on a warmed-up basis—that is, as they would appear in actual applications. Warm-up does not affect the bipolar devices, but because of power dissipation, the chip temperature of the FET-input LF411 is more than 10°C higher than the ambient, thus doubling the FET input currents. This phenomenon also causes the circuit's bias current to reach more than 50 nA at 125°C.

As can be seen, the OP-07 has the least voltage noise, but the LT1008 is only slightly higher, thanks to its lower operating current. The LM11 trails with 10 times greater noise.

For the other parameters, the LT1008 is the leader, with the OP-07 second. The common-mode and power-supply rejection ratios of the LT1008 are at least five times better than the others (with the exception of the LM11's CMRR, compared with which the improvement is 1.5 times). Note that even with the higher gain, the LT1008 can drive a 5-mA load, but the LM11 cannot. To top it off, the improvement in supply current of the LT1008 over the OP-07 and LF411 is particularly striking.

Frank Goodenough

Comparing precision op amps

	LT1008C	OP-07C	LF411AC	LM11C	LM308A
Input-offset voltage (μV)	120*	150	500	600	500
Input-offset voltage drift with temperature (μV/°C)	1.5	1.8	10.0	5.0	5.0
Input offset current † (pA)	100	6000	200	10	1000
Input bias current † (pA)	100	7000	400	100	7000
Voltage noise, typical 0.1 to 10 Hz (μV pk-pk) At 10 Hz (nV/$\sqrt{Hz}$)	 0.5 17	 0.35 10.5	 2.5 55	 6.0 180	 0.9 30
Voltage gain (V/mV) R_L = 10 kΩ R_L = 2 kΩ	 200 120	 120 120	 N.s. 50	 100 N.s.	 80 N.s.
Common-mode rejection ratio (dB)	114	100	80	110	96
Power-supply rejection ratio (dB)	114	90	80	100	96
Supply current (mA)	0.6	5.0	2.8	0.8	0.8

Notes: V_S = ±15 V, T_A = 25°C.
All specifications except voltage noise have been taken directly from the manufacturers' data sheets and are guaranteed unless noted as typical. Highlighted areas represent the salient characteristics of the earlier devices. The published 100-piece prices for all five op amps are between $2.80 and $3.90 (TO-5 package)
N.s. = not specified *LT1012C guarantees 50 μV. †Warmed up.

zener zap circuitry. The output- power-boosting network enhances load drive capability by sensing the output vertical-pnp load current and injecting additional base drive to the pnp when needed. This boost is accomplished without increasing idling current, thereby maintaining the low supply current of the 1008/1012.

Active filter applications abound, and some, such as for a high-resolution electronic scale have contradictory needs—a long time constant but fast response. The 1008/1012's combination of low bias current, low drift, and high common-mode rejection serves this application well. In electronic scales it is desirable to acquire the weight signal quickly, but long-time-constant filtering is mandatory to eliminate noise. The noise is due to vibrations transmitted through the floor or actual motion on the weighing platform. Moreover, the filter absolutely must not introduce any significant dc error into the signal path.

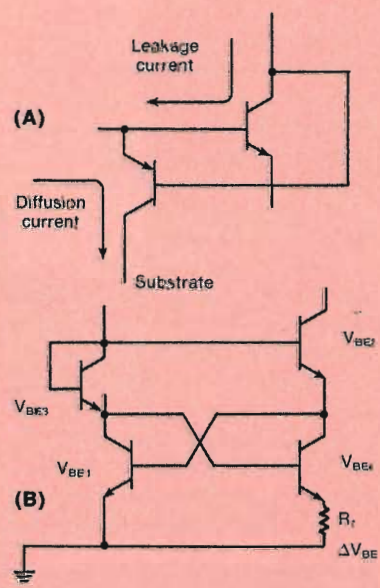
A cross between a sample-and-hold amplifier and a filter does the job with a 1012 (Fig. 2a). With no weight on the scale, the circuit input and output are zero. When a weight-related input appears, comparator C_1's output goes low, biasing the optically driven FET switch on. That allows the 1-μF capaci-

Current leakage and current regulators

Leakage current at high temperature is easier to control in an integrated circuit than in circuits made with discrete transistors. The reason is that critical nodes can be made small (in area), keeping junction leakage to a minimum. Furthermore, since these IC transistors are really four-terminal devices (the fourth terminal is the substrate), optimum bias voltages virtually eliminate leakage currents. Figure A shows the equivalent circuit of an npn transistor for a typical IC, indicating both the leakage current and the compensating diffusion current.

In actuality, the pnp transistor is not a separate device from the npn. The base region of the latter is the emitter of the former and the collector region of the npn transistor is the base of the pnp transistor. Therefore the collector base leakage of the npn transistor will appear as leakage current at the input terminals of an op amp, degrading bias current with high temperature. Current through the pnp transistor (diffusion current) can be used to shunt this leakage to the substrate. This current is controlled by the collector-to-base bias voltage on the npn transistor, approximately 0.2 V minimizes leakage.

Bias current compensation also helps to keep input currents low over a wide temperature range. It is done in the LT1008/1012 within a feedback loop (Fig. B), in contrast to the scheme used in the OP-07. As long as the leakage from the compensation transistor is the same as that from the input devices, the feedback loop will compensate for them.



The bias network used in the LT1008/1012 is also interesting because of its simplicity and performance. All of today's high-performance op amps are expected to operate over a wide supply range with no performance change. That mandates some type of regulator loop for the internal bias circuitry to regulate against supply voltage variations. Moreover, in a low-power op amp, very little power can be spared for the bias loop.

The regulator used in the 1008/1012 keeps the output constant for an extremely wide range of input currents (Fig. B). Further, the temperature dependence of the output current is proportional to absolute temperature, compensating for the input stage transconductance. Although four transistors are used in the loops, the output current depends only on the difference in transistor areas and is given by $I_{out} = \Delta V_{BE}/R_1$, where ΔV_{BE} is the sum of the emitter-base voltages around the loop. That is, voltage change $\Delta V_{BE} = \Delta V_{BE1} + \Delta V_{BE2} - \Delta V_{BE3} - \Delta V_{BE4}$.

Emitter-base voltages V_{BE1} and V_{BE3} are both proportional to the input current and subtract from each other. Emitter-base voltages V_{BE2} and V_{BE4} are proportional to the output current, and they also subtract from each other. The only fraction of voltage that does not cancel is that generated across R_1 by area differences. Now, the only requirement for the input current is that it must be greater than the output current divided by the current gain of these transistors.

Robert Dobkin, Vice President Engineering
Carl Nelson, Manager Design Engineering

Reference:
1. C. T. Nelson, "A 0.01% Linear Instrumentation Amplifier," *ISSCC Digest of Technical Papers*, pp. 134-135, February 1980

tor to charge rapidly through resistor R_2 toward the input. When the 1012's output exceeds the potential at C_1's negative input, C_1 unclamps and the switch turns off. Now the capacitor must finish charging through the combination of resistors R_1 and R_2. In this manner, the circuit rapidly acquires almost all of the input amplitude before switching into the long-time-constant filter mode. The 1012 eliminates loading on the capacitor without introducing error.

The circuit's output slews to within 75 mV of final value before switching into the filter mode, thus permitting it to settle quickly. (Fig. 2b). Comparator C_2 resets the capacitor when the platform weight is removed by turning on when the input goes toward zero. C_2's output cannot pull low under any other conditions because of the deliberate offset introduced by connecting the null pin to V^+.

A charge-pump voltage-to-frequency converter circuit takes full advantage of the 1008 working as an integrator (Fig. 3a) Although charge-pump circuits provide high linearity and stability, their transfer function often degrades at low frequencies because they employ simple RC integrators. In this circuit, a high-grade integrator (resistor R_1-R_2, capacitor C_1, and amplifier A_1) maintains linearity in the low range providing the 120-dB dynamic range of 0.01 to 10 kHz.

A positive voltage input applied to the circuit causes the 1008's output to integrate negatively. When its output equals the 1.2-V potential of the LT1004 reference, the output of amplifier A_2 goes negative, discharging the 1000-pF capacitor, C_2, and injecting a fixed quantity of charge into the 1008's summing junction, D_6. Capacitor C_3 and resistor R_3 supply positive feedback to A_1 to ensure a complete discharge of C_2. This charge-pump action resets the integrator.

When the positive feedback ceases, the integrator begins to ramp again and the output of A_2 is saturated high, allowing C_2 to recharge and thereby readying the circuit for the next discharge cycle. The zener diode bridge (D_1-D_5) provides stable saturation limits, and the diodes at D_6 furnish current steering and compensation for bridge temperature shifts. The 311 type comparator ensures start-up and recovery from input overdrive by pulling D_6 low if the output of A_1 ever exceeds its normal range.

The 1008's low offset voltage and bias current yield 100 dB of input signal range without offset trimming. An additional 20 dB may be obtained by using the optional trim (resistors R_4 and R_5). To trim the circuit, 10 V is applied at the input and the 10-kΩ input potentiometer (R_1) is adjusted for 10.000 kHz out. If a still wider signal range is desired at the low end, it can be achieved by applying 10 μV to the input and trimming the 50-kΩ pot (R_5) for 0.01 Hz out. The transfer nonlinearity of the circuit is 0.01% over its complete dynamic range of 1 million to 1.

Logarthmic amplifiers are used for dynamic range compression at dc in low frequency instruments such as CAT scanners and spectrophotometers. They provide conformity to a perfect log curve to within 1% over a dynamic range of 120 dB, or 1 million to 1 when operated with a current input signal. However most available modular or hybrid devices are limited by the amplifier's offset voltage to a range of about 10,000 to 1 when the input signal is a voltage, and even then trimming is required. In the circuit of Fig. 4 the low offset voltage of the 1012, combined with its low bias current, provides voltage logging to 99% conformity with input signals of 10 mV to 10 V (80-dB dynamic range). Moreover, trimming is not required and the input resistance is still 10 kΩ. If the offset voltage of the amplifier is trimmed, a dynamic range of 100 dB can be obtained.

Like most logarithmic circuits, this one is based on the inherent logarithmic relationship between a bipolar transistor's collector current and its base-emitter voltage, V_{BE}. Q_{1A} functions as the log transistor here and is enclosed within A_1's negative feedback loop, which includes the gain-setting divider (R_2-R_3). The input to the circuit (E_{in}) forces the output of A_1 to achieve whatever value is required to maintain its summing junction (pin 2) at zero potential. Because Q_{1A}'s response is dictated by the logarithmic relationship between the collector current and V_{BE}, the output of A_1 will be the logarithm of the circuit input. Amplifier A_2 and Q_{1B} provide compensation for Q_{1A}'s V_{BE} temperature dependence. The negative feedback of A_2 forces Q_{1B}'s collector current to equal the 10-μA current established by the LT1004 reference diode and the 124-kΩ resistor (R_4). Since Q_{1B}'s collector current cannot vary, its V_{BE} is also fixed. Under these conditions, only Q_{1A}'s V_{BE} will be affected by the input.

Without some form of compensation, the scale factor will change with temperature because of thermal shifts in Q_{1A}. The simplest solution is to have the 1-kΩ resistor (R_3) vary with temperature. For the device shown, compensation is within 1% over −25° to +100°C. The R_2-R_3 divider sets the circuit's gain to provide 1 V out for each decade change in the input voltage. With zero in, the output is 100 mV.□

How useful?	Circle
Immediate design application	541
Within the next year	542
Not applicable	543

Charge-nulled CMOS switch lets op amps tackle precision analog tasks

A dual DPDT switch aimed at switched-capacitor designs ushers in a new age of instrumentation amplifiers, analog multipliers and v-f converters.

Converting differential signals into single-ended form is an essential ingredient of analog signal processing. However, accurately extracting those single-ended signals in the presence of a large common-mode potential proves a tough job. Though several types of amplifiers have been assigned the job, they serve as stopgap measures.

On the one hand, instrumentation amplifiers can afford the necessary degree of precision, but are relatively expensive. Isolation amplifiers, on the other hand, can allow desired signals to be extracted in the presence of large common-mode voltages; however, their relatively large gain drift and inherent nonlinearity limit their ultimate precision.

A CMOS chip housing two double-pole, double-throw (DPDT) switches, designated the LTC1043, virtually eradicates those difficulties. When accompanied by two standard small-signal capacitors, each of its two sections (Fig. 1) turns a high-performance op amp into an instrumentation amplifier that rivals or beats the performance of today's chips or hybrids.

The value of the switch does not stop at instrumentation amplifiers. Instead it extends to high-accuracy analog designs like multiplier-dividers, voltage-to-frequency and frequency-to-voltage converters, and voltage inverters.

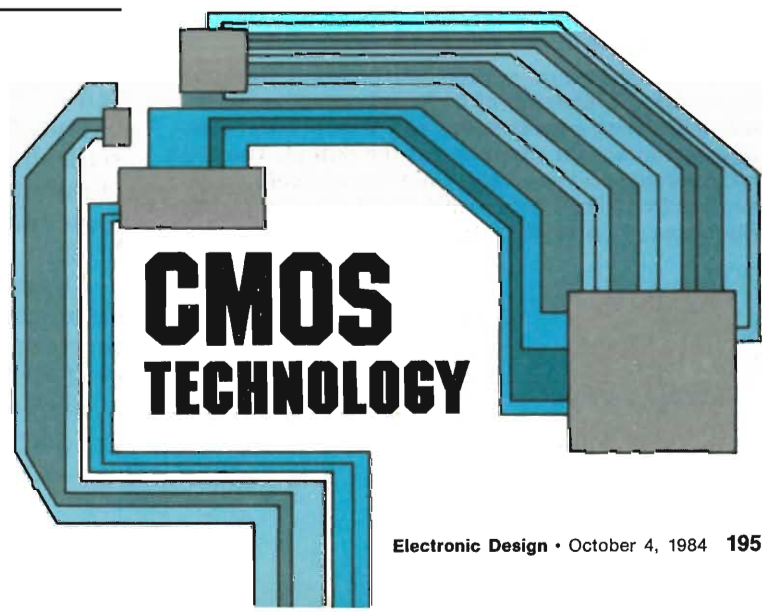
Reining in the charge

The switch's appeal lies in its ability to prevent leakage currents from appearing at the output, thereby minimizing sampling errors (see "Compensating for the Errors," p. 197). It

Nello Sevastopoulos and **Jim Williams**
Linear Technology Corp.

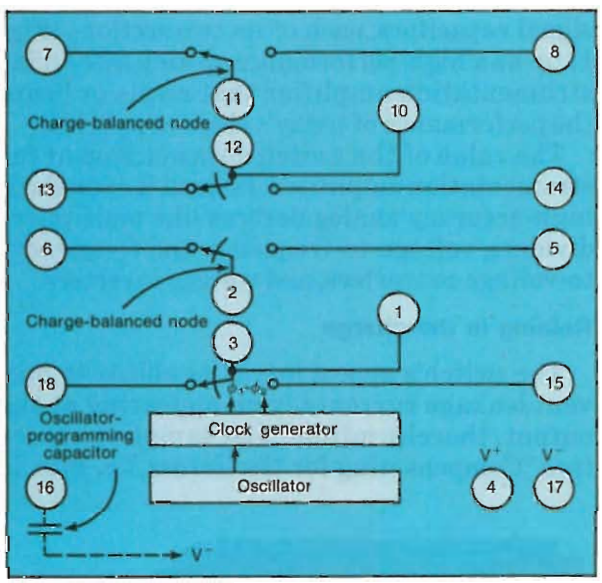
Nello Sevastopoulous runs the analog MOS design group at Linear Technology Corp. Previously he was head of the MOS IC design section at National Semiconductor. He holds an MSEE degree from Santa Clara University.

Jim Williams is a staff scientist at Linear Technology, specializing in analog circuit design. Before that, he was the applications manager for linear ICs at National and a consulting engineer for the Massachusetts Institute of Technology.



essentially serves as the front end for a switched-capacitor instrumentation amplifier. Although its on-resistance is not notably superior to that of existing CMOS switches, its charge-balancing circuitry dampens the effects of stray capacitance. Thus the device meets its primary objective: transferring charge with precision.

Based on a flying-capacitor technique, the DPDT switch helps create an economical circuit for converting differential into single-ended signals. In that type of configuration, a sampling capacitor, C_S, alternately switches between the output of a balanced bridge that represents the signal source and a holding capacitor, C_H. (Alternate arms of the bridge are connected to the positive rail and ground.) After a number of commutation cycles, the voltage across C_H equals that across C_S. Any common-mode component is removed.



1. The LTC1043 dual-section DPDT switch, designed for switched-capacitor circuits, is compensated to eliminate stray capacitances and thus prevent leakage currents from appearing at the output. The MOS chip includes a two-phase clock for switching each section in a break-before-make fashion at commutation rates of up to 200 kHz.

Controlling the break-before-make action of each switch is an internal oscillator, which drives a two-phase nonoverlapping clock generator working at a free-running frequency of 200 kHz. The rate can be adjusted from several hertz to 200 kHz with an internal capacitor. The oscillator also can be disabled and the switch driven by an external clock, if desired.

Meeting the specs

To demonstrate its prowess with analog tasks, consider the LTC1043's role in building an instrumentation amplifier for a transducer-fed system (Fig. 2). The simple configuration matches the best hybrid or monolithic amplifier in its low offset, low gain drift, high common-mode rejection ratio, and high linearity. Key performance specifications vary with the output instrumentation amplifier chosen (see the table, p. 198).

The stage gain is set by resistors R_1 and R_2. Capacitor C_F determines the roll-off (frequency) response of the amplifier, the control of which conventional instrumentation amplifiers cannot achieve with external components. The highest precision is obtained through a low oscillator frequency, typically 300 to 1000 Hz. That rate minimizes the number of switch transitions, reducing the effects of charge-injection residues. Typically, the charge transfer accuracy will be within a few parts per million. The maximum linearity error is about 2000 ppm at a sampling frequency of 200 kHz.

Note that the switch chip behaves like a switched capacitor low-pass filter, with the commutation frequency controlling the roll-off. The stage thus filters the acquired signal before it is amplified, thereby preventing potential nonlinearities from appearing at the output. Additionally, ac common-mode signals see a short circuit at the input and will thus be eliminated from the output if the input source impedances are balanced (as in a transducer bridge).

An expansion of that idea employs a chopper-stabilized amplifier (the LTC1052) that has better dc specifications than current units. Half the DPDT switch is set up with a diode to create a small negative voltage drop (Fig. 3). As a result, the amplifier is biased in class A, allowing

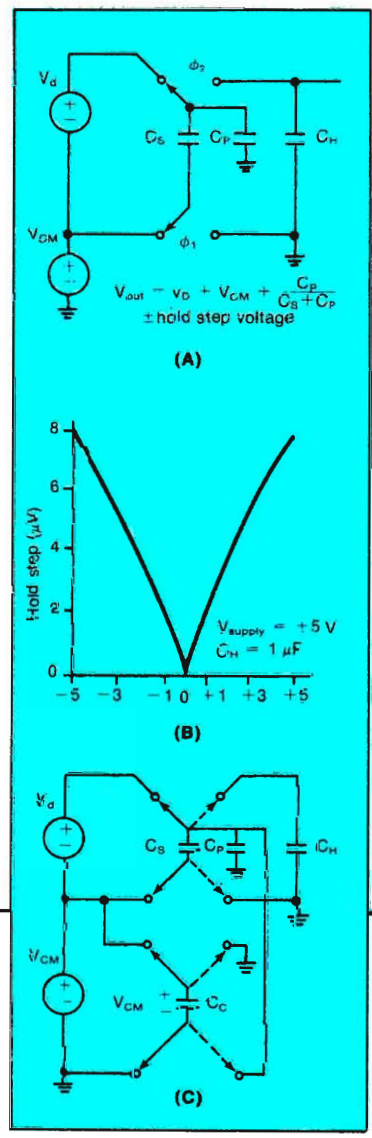
Compensating for the errors

A proprietary silicon-gate process deserves much of the credit for the dual DPDT switch's ability to manipulate charges without introducing significant errors. The process, which makes the gate structure retain its symmetry with respect to source and drain, ensures that the overlap capacitance between the gate and the drain and between the gate and the source of identical p- and n-channel transistors forming a CMOS switch is virtually identical. As a result, hold-step errors become dependent only on the amount of charge injected into the channel. Also, errors are virtually canceled when the sample differential voltage is nearly zero (see B). Such a technique gives the chip a common-mode rejection ratio that approaches infinity at low frequencies and has nearly ideal gain linearity. Additionally, it requires no external precision capacitors.

It is virtually impossible to build a high-accuracy flying-capacitor circuit with conventional switches, which are prone to two basic sources of error. First, consider the error associated with measuring differential voltages. During the sampling mode (see A), the charge placed on sampling capacitor C_S is equal to $C_S V_d$. The switch's parasitic capacitance, C_P, however, charges to the sum of the common-mode voltage (V_{CM}) and the differential voltage (v_D). (Note that one end of C_P is virtually grounded.) The excess charge placed on C_P is thus equal to $C_P V_{CM}$ and is shared equally by C_P and C_S during charge-transfer phase. Initially, then, the voltage placed on hold capacitor C_H is:

$$V_D + V_{CM}[C_P/(C_S + C_P)] \pm \text{hold-step voltage}$$

A second error voltage is added when the switches toggle (off-state to on-state) to again sample the differential voltage. During that interval, an additional error occurs that is similar to the hold-step error observed in sample-and-hold circuits. In conventional CMOS switches, this error is due mainly to the mismatch of the gate-to-drain/source overlap capacitance. Additionally, the channel charge injected into the drain/source during a switch's turn-off contributes to the hold-step error.



Parasitic capacitances are not easy to cancel, since they are essentially the sum of error capacitances of various sources. The most important ones to consider are the junction capacitances of the switches. By means of special MOS transistor geometries, however, the internal junction capacitance of the switches is made almost constant, permitting internal compensation of C_p with capacitor C_C (see C). This (internal) capacitor's value is equal to that of the switch's junction capacitance C_P and virtually cancels the V_{CM} error. (The V_{CM} term becomes $[V_{CM}(C_P - C_C]/[C_S + (C_P - C_C)] = 0$.) During the circuit's sampling mode, C_C samples the common-mode voltage. Then, during the charge-transfer mode, C_C's polarity reverses. Because C_C is essentially connected in parallel with the switch's junction capacitance, the newly negative charge on C_C cancels the positive charge on C_P.

As for the interpin capacitances within the dual in-line package, they are not canceled but their effects are eliminated with a dummy pin, which places any additional capacitance across the nonprecision sampling capacitor C_S. The pc board's stray capacitances are also referenced in parallel with C_S by adding a shield under the sampling capacitor and tying it to the dummy pin.

CMOS Technology: Dual switch chip

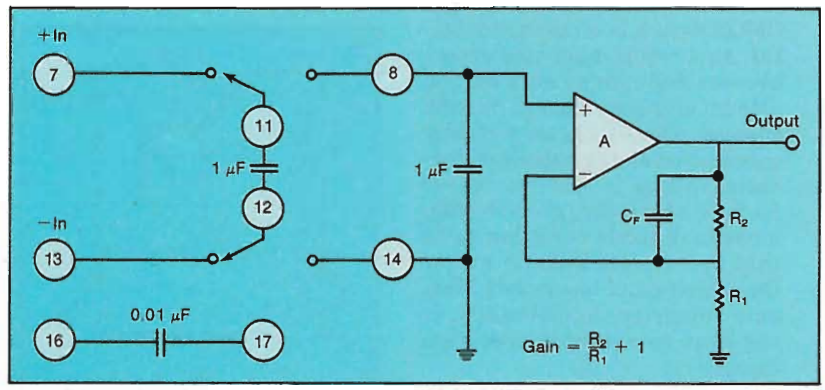
its output to swing fully to zero. As for the performance of the circuit, input offset is less than 3 μV. Drift is below 0.05 μV/°C, and common-mode rejection ratio goes beyond 120 dB from dc to 20 kHz.

Measuring small signals

The LTC1043 also makes an excellent choice in transducer signal conditioning (Fig. 4). Here, the thermistor network is offset with respect to 0°C so that it can work as an accurate subtraction device. Thus, 0°C corresponds to a voltage of 0 V at the output.

Turning a differential signal into a single-ended one, the switch chip extracts the difference between thermistor T's output and a scaled reference voltage. The output amplifier provides calibrated gain, so that the circuit's output voltage will correspond directly to temperature.

Calibration is easy. First the potentiometer is set for a voltage of 1.068 V at pin 7 of the switch chip. Next, pin 13 is shorted directly to the reference's output and the 100°C trim potentiometer is set for an output voltage of 0.2527 V. The circuit is accurate to ±0.25°C over



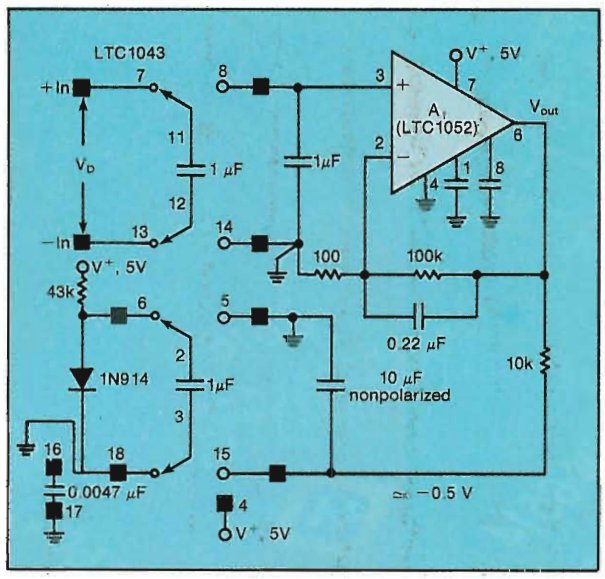
2. The switch chip and two standard signal-handling capacitors turn a high-quality op amp into a precision instrumentation amplifier that converts differential into single-ended signals. The commutating frequency should be below 1 kHz for best performance. Stage gain is set by two resistors. The feedback loop that includes capacitor C_F gives a degree of external control of the op amp's roll-off characteristics.

Worst-case performance of instrumentation amp

Parameter	LT1001/LT1002	LT1012	LT1013/LT1014
E_{OS}	15 μV	35 μV	150 μV
$E_{OS}/\triangle TC$	0.6 μV/°C	1.5 μV/°C	2 μV/°C
I_B	2 nA	100 nA	20 nA
Common-mode rejection ratio	> 120 dB	> 120 dB	> 120 dB
Gain drift	1 ppm/°C typ*	1 ppm/°C*	1 ppm/°C*
Linearity	1 ppm	1 ppm	1 ppm
Power supply	±5 to +15 V, GND	±5 to +15 V, GND	+5 V, GND to ±15 V

*Limited by gain-controlling-resistors

CMOS Technology: Dual switch chip



3. For especially good performance down to dc, a chopper-stabilized circuit fills the bill. Half the DPDT switch and a diode develop a small negative voltage that biases the amplifier, thereby permitting the circuit's output to swing fully to zero.

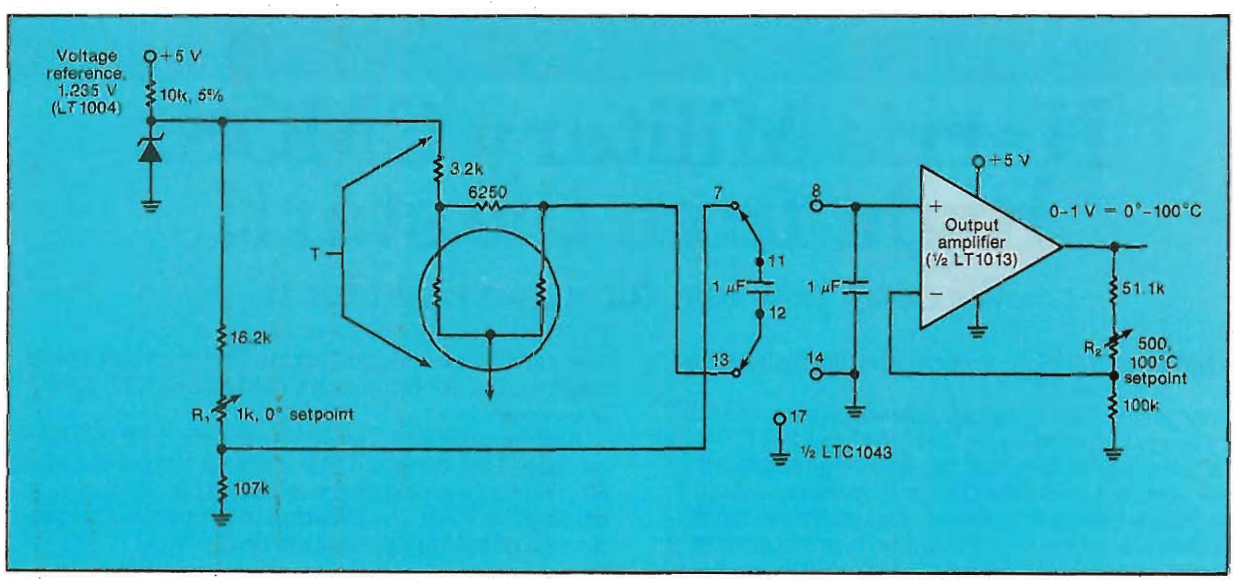
a temperature range of 0° to 100°C.

The LTC1043 can also fit into a voltage-controlled current source having both source and load referred to ground (Fig. 5). A simpler and more precise circuit than the commonly employed Howland configuration, it requires only one precision component—the load resistor. Moreover, it can drive transducers and current-loop transmitters in industrial control systems.

Better power sources

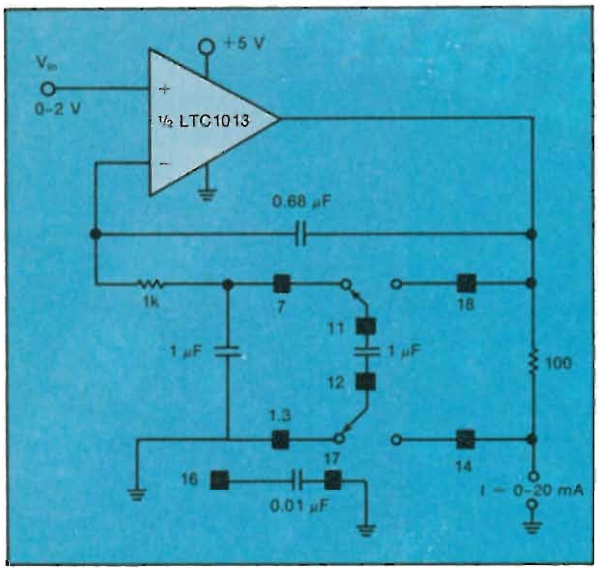
The amplifier in the configuration drives current into the grounded load through the 100-Ω resistor. The 0.68-μF capacitor and the 1-kΩ resistor form a dominant feedback loop that is unconditionally stable. If desired, the remaining section of the DPDT chip can be placed ahead of the amplifier, creating a fully differential voltage-controlled input.

A scheme like that proves handy for offsetting the amount of current in the loop or when the control voltage is not referred to

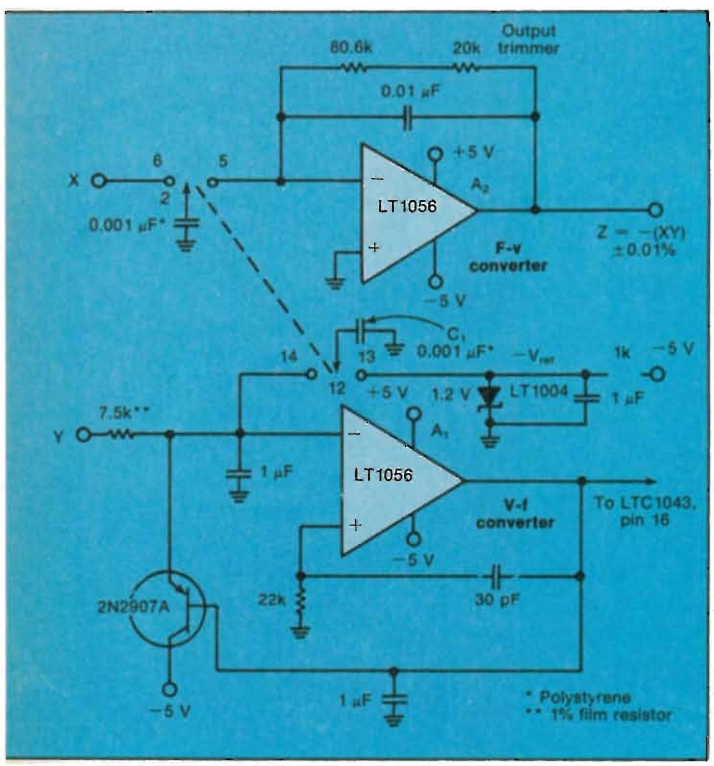


4. The DPDT switch chip is well-suited to use in low-level transducer circuits. Here a voltage-subtraction circuit permits a thermistor network to deliver a voltage that is directly proportional to the temperature in degrees Celsius. Each easily calibrated unit is accurate to within ±0.25°C over 0° to 100°C.

CMOS Technology: Dual switch chip



5. A voltage-controlled current source needs only one precision component—a load resistor. The circuit is unconditionally stable for input voltages between 0 and 2 V, delivering an output of 0 to 20 mA.



6. Along with voltage-to-frequency and frequency-to-voltage converters, the LTC1043 helps build an analog multiplier that is accurate to 0.01% over the input range of −5 to +5 V. Linearity is 0.005%, and gain drift is 20 ppm/°C.

ground. The accuracy and stability of the circuit is almost entirely dependent upon the characteristics of the 100-Ω resistor.

Voltage-to-frequency and frequency-to-voltage converters capitalize on the LTC1043's ability to manipulate charge, as in an analog multiplier with 0.01% accuracy (Fig. 6). Since the circuit is more accurate than any commercially available analog multiplier, it could be put to work linearizing a bridge or transducer. In fact, it is extremely useful in all but the most stringent applications.

Making an easy conversion

In this circuit, the v-f portion is biased from the Y input. The X input establishes a voltage reference for the f-v portion. Thus the value of X controls the signal path's attenuation from the Y input to the Z output.

In operation, the X and Y input voltages produce a summing current at the input to A_2. Assume that Y is initially zero, and A_1's inverting input is below ground. Therefore the output of A_1 is high. As a result, the switch's oscillator is enabled, and pin 12 of the switch is connected to pin 13. Thus the 0.001-μF capacitor, C_1, charges to $-V_{ref}$. When the inverting input rises above ground, A_1's output flips, driving the switch's clock pin low (the transistor circuit is a start-up loop that ensures switching).

That action connects C_1 to pin 14, pulling charge from the 1-μF capacitor connected at A_1's input and lowering A_1's input voltage. The RC network at A_1's noninverting input provides hysteresis to allow complete charging of the 0.001-μF capacitor at pin 12. The process repeats, with the frequency of oscillation of this loop being directly proportional to the voltage at the Y input (i.e., the discharge time of C_1). As for performance, this circuit provides 0.005% linearity. Scale drift is 20 ppm/°C.

To calibrate the conversion, the X and Y inputs should be shorted, 0.7321 V applied, and A_2's output trimmer adjusted for an output voltage of exactly 3 V. □

How useful?	Circle
Immediate design application	547
Within the next year	548
Not applicable	549

Nanoampere comparator IC with stable offset manages inputs unaided

A dual comparator chip enlists a discrete time-sampling scheme to attain fully differential inputs, high gain, and a precisely fixed offset.

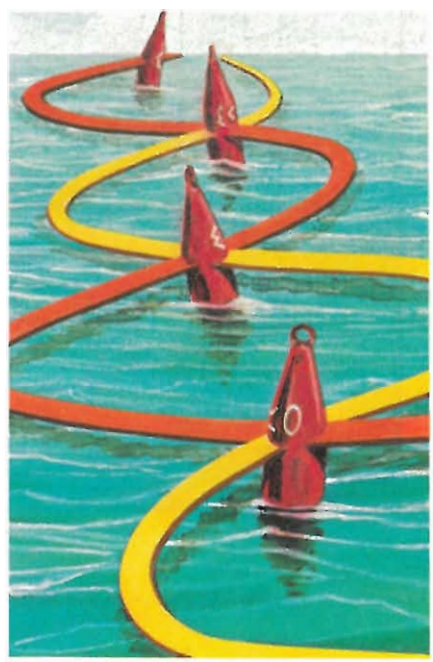
Jim Williams and **Tom Redfern**
Linear Technology Corp.

Jim Williams is a staff scientist for Linear Technology, in Milpitas, Calif., where he has worked for about three years. He defines products and tracks them through the breadboard stage.

Tom Redfern is the CMOS design manager at Linear Technology and designed the LTC1040 comparator. Among other accomplishments, he is responsible for enhancing the design of two popular circuits—the IC7660 voltage converter and the ICL7652 chopper-stabilized op-amp. His BSEE and MSEE are from Stanford University.

Despite their appeal, voltage comparators have not kept pace with the complex needs of many applications. Monitoring and process control, in particular, often call for low power comparators to ensure portability yet still require high gain for transducers, as well as differential inputs for bridges and other floating sources. Adding the circuits to deliver these features is not just inconvenient; when power consumption is at stake, as in battery-operated equipment, extra components are anathema.

Engineers are delivered from that dilemma by the LTC1040 CMOS dual comparator, which resolves all those issues—drain, gain, and differential inputs—on a single chip. The device is intended for such tasks as detecting faults, sensing limits, and managing process-control loops. In each case, low power and stability are generally more important than speed.



In a departure from conventional linear design, the chip uses switched capacitors and discrete time sampling to turn it into a virtual power miser. When capturing 1 sample a second, say, each comparator draws an average of only 48 nA from a 5-V dc supply. And although the actual current drain will vary with the application, it is often less than a battery's self-discharge rate.

From a system standpoint, the dual comparator keeps an even tighter rein on power by obviating the need for much, if not all, standard interface circuitry. Each comparator's input consists of two fully differential pairs that unfailingly sense voltage variations to within 500 μV. With that unvarying sensitivity, each comparator can process low-level signals directly—that is, without external dc gain stages.

Moreover, the single offset specification alone accounts for all the effects of time, tempera-

Dual comparator chip

The switch to capacitive inputs

Switched-capacitor comparators have been employed in MOS analog-to-digital converters for the last decade and are generally acknowledged as the best way to implement a comparator in CMOS. Nevertheless, the LTC1040 is the first instance of such a comparator being offered as a discrete component—designed for low power and high precision.

The basic action of a switched-capacitor comparator is to sum the charge at a virtual ground node. Analogously, an op amp also sums currents at one of its virtual ground points, the inverting input. In the op amp, resistors convert input voltages into currents; in switched capacitors, the capacitors convert differential voltages into specific charge levels.

The capacitive input structure has at least two important advantages over the differential amplifier's resistive summing method. It can be driven by a high-impedance source without suffering from errors due to loading. (However, there must be sufficient time for the capacitors to fully charge.) Also, charge can be subtracted as well as added—the resistor analog only adds.

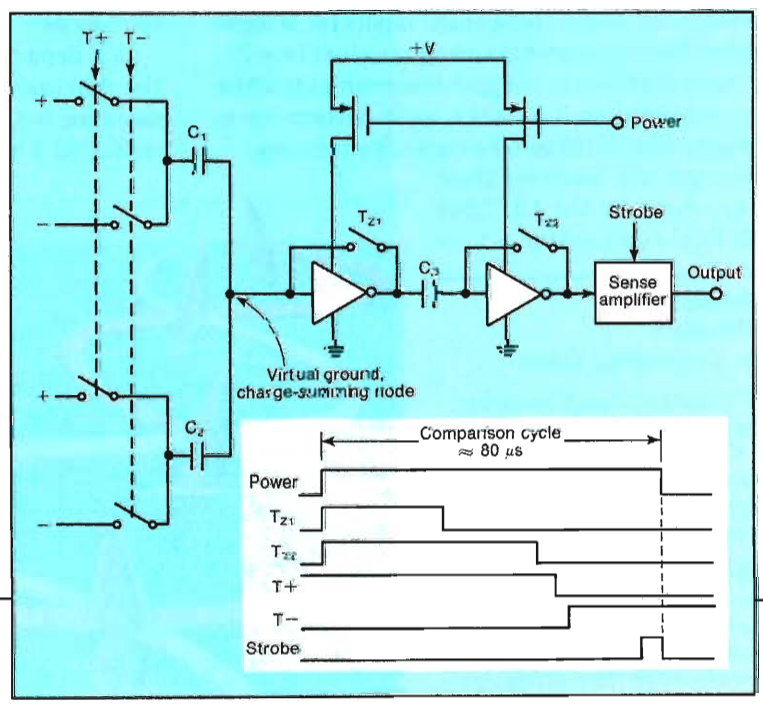
The comparator's guaranteed minimum offset voltage of 500 μV and its $\pm 0.1\%$ accuracy over a $-55°$ to $+125°C$ temperature range are just two proofs of the excellence of its proprietary silicon-gate CMOS capacitive structure. Traditionally, offset errors result when a charge is injected from internal MOS switches. They also occur, but to a lesser extent, with this comparator's self-aligning silicon gate.

What's more, the summation accuracy is fixed by the ratio of the input capacitors, and integrated MOS capacitors are the most accurate IC components. Not only is the tolerance of the ratio well controlled, but each capacitor's absolute value, as well as the change in its input error due to time, mechanical stress, and voltage are far superior to any other component.

Further reducing the sources of offset error, and contributing to the comparator's consistently high performance, are its chopper-stabilized input and autozeroing gain stages. For the most part, these techniques null the effects of changes in temperature, gain, and power supply and input common-mode voltages.

Before the comparator begins sampling any input voltages, its two gain stages are separately zeroed, so that the second stage eliminates the charge injection error of the first (see the figure). Time-zero switches, T_{Z1} and T_{Z2}, start in the closed position, shorting the first and second gain stages, respectively, and giving the comparator time to settle. Then T_{Z1} opens and injects a charge into the input capacitor structure. That charge causes an error, but because T_{Z2} stays closed, it also appears at the coupling capacitor, C_3.

Next, T_{Z2} opens. This injects a charge into C_3 and results in a voltage across it that determines the final comparator offset. This error, as reflected back to the input, is reduced by the open-loop gain of the input stage.



ture, and common-mode and power-supply voltages. Its unprecedented stability grows out of the chip's reliance on capacitive-switch technology. Among other advantages, this approach makes the input stage into a chopper-stabilized amplifier, which automatically corrects for any parametric changes (see "The Switch to Capacitive Inputs," opposite).

The 500-μV offset means that when the sum of a comparator's differential inputs is more than 500 μV, its output goes high. Alternatively, the output is low when the sum is less than -500 μV. As a result, precise analog subtraction, as well as addition, is a routine matter for the comparator, even if the input voltages are referenced to a point other than ground.

At its outputs, the chip delivers four TTL- and CMOS-compatible signals: one for each comparator, A and B; the NORed results of A and B, $(\overline{A+B})$; and On/$\overline{\text{Off}}$. The NORed output simplifies designing window comparators; the On/$\overline{\text{Off}}$ pin lends itself to upper- and lower-limit, or "bang-bang," controllers.

A power-pulsing plus

A pulsed power signal is another of the chip's system-oriented features. It controls, and thereby reduces, the average power consumed by external transducer circuitry. When a comparator turns on, the pulsed power (V_{PP}) output connects to the positive supply voltage. At the end of the 80-μs sampling period, the link is severed, removing the power. Thus the power shunted to a transducer bridge, resistor divider, voltage reference, or other transducer element is locked to a comparator's actions and applied only when needed.

Accepting common-mode voltages up to the level of the supply rails puts the chip in a class by itself. That capacity, wed to the IC's differential inputs, makes measuring load currents simple and straightforward. One way to monitor a circuit's load current, for example, is by connecting the comparator to the differential voltage across a 0.1-Ω resistor in series with either the positive or negative supply rail (Fig. 1). That voltage is contrasted to a ground-referenced 10-mV source, and when the load current exceeds a specific value, in this case 100 mA, the comparator output goes high.

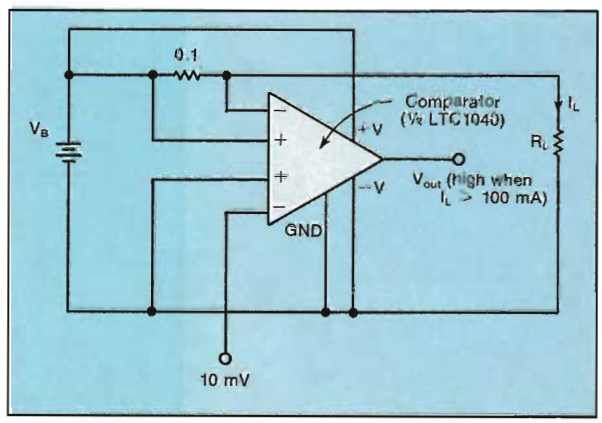
Although the chip can be powered from +5 V dc ($\pm$5%) alone, it also accepts a negative supply voltage to accomodate negative inputs or common-mode voltages. The only restriction is that the total supply voltage, from +V to $-$V, must not exceed 16 V.

Even all of these striking features pale when the device's low power consumption is considered. What keeps that demand so miniscule is an intermittent supply-current flow. When the comparators are in action, the IC typically draws 1.2 mA from a +5-V dc supply. Once the comparison is complete, an internal sense amplifier is strobed and the chip stores the results in its output stage. As soon as that is done, the chip shuts down, drawing virtually no current.

As mentioned, the entire sampling and comparing cycle takes roughly 80 μs. Thus the 1.2-mA current flows for only that time, making the average current equal to 1.2 mA multiplied by 80 μs multiplied by the sampling frequency (in hertz). Thus it is proportional to the sampling frequency, or strobe rate.

A starvation diet

In applications marked by slowly varying parameters, like temperature monitoring, measurements need be made only occasionally, and power consumption can be reduced to an arbitrarily small amount. As noted, in battery-backed setups, it is likely that the power needed by the comparator would be less than the battery's self-discharge rate. For instance, a strobe rate of one sample every second with a 5-V dc



1. The LTC1040's two sets of fully differential inputs and its common-mode rating up to the supply rails simplify measuring load currents. One input keeps tabs on the voltage across a 0.1-Ω current-sensing resistor. The other input is connected to a ground-referenced 10-mV source. The comparator's output goes high when the load current exceeds 100 mA. A negative supply voltage is optional.

Dual comparator chip

supply subsists on an average power of 0.48 μW, as the following formula shows:

$$P_{average} = 5\,V \times 1.2\,mA \times 80\,\mu s \times 1\,s$$
$$= 5\,V \times 9.6 \times 10^{-9}\,A = 0.48 \times 10^{-6}\,W$$

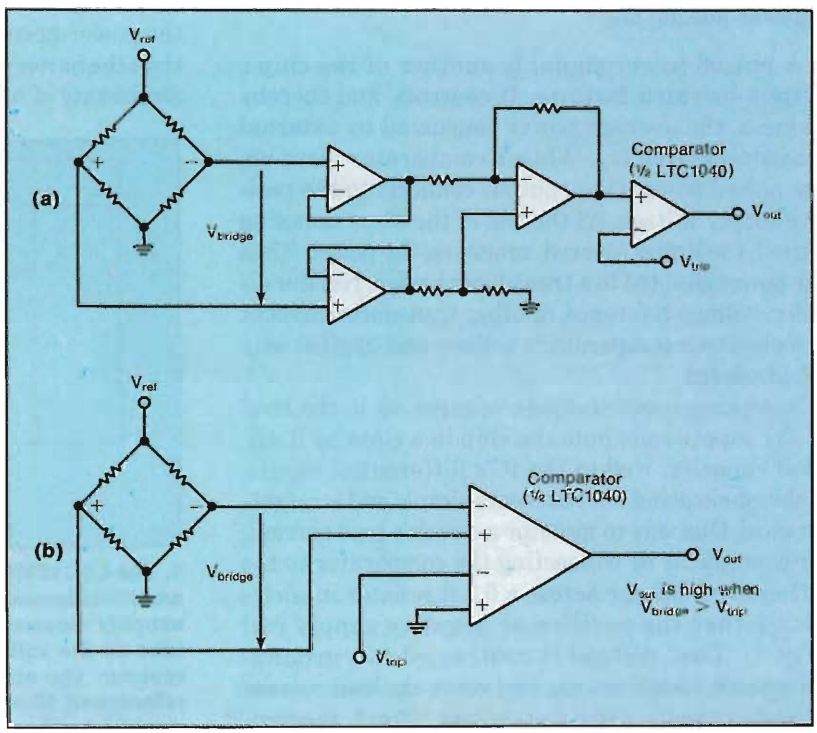
Such low power consumption suits the IC to completely self-contained, internally powered systems. Remarkably, a temperature controller packaged with its own lithium battery and using up only 0.48 μW would stay in service for 20 years.

Indeed, at extremely low sampling rates, the chip's comparator logic is not the chief consumer of power. The IC's on-board oscillator, which strobes the two comparators, and the positive power supply's leakage to ground through the chip, draw the largest shares of current. Consequently, a true picture of the chip's current draw must take these two factors into account.

The power consumed by the relaxation-type oscillator is dissipated by an external resistor, R. In operation, a capacitor charges up through R to a voltage, V. When the capacitor voltage reaches V, it turns on a transistor, in turn discharging the capacitor. As the capacitor discharges, the transistor shuts off. The capacitor starts charging again and the cycle repeats itself. The power consumed by the resistor is given by $P_R = (V/2)^2/R$. For a 10-MΩ resistor and a 5-V supply, the dissipated power is 0.625 μW, or 30% more than that of the comparator circuit.

But it is the leakage current, guaranteed to be 0.5 μA or less, that contributes most to the power consumed by the comparator and the oscillator. Nevertheless, the sum of all these factors is still less than the battery's self-discharge rate.

Like the chip's extremely low power needs, another feature that sets it apart from the pack is its high-impedance, high-gain differential inputs. These instrumentation-type inputs eliminate the need for additional gain stages and simplify links to transducers, bridges, and other sources that are not refer-



2. Conventionally, detecting when the voltage across a floating source, like a bridge, exceeds a chosen level demands three op amps (a). Because the LTC1040 accepts differential voltages directly, it needs no op amps to make the same measurement (b).

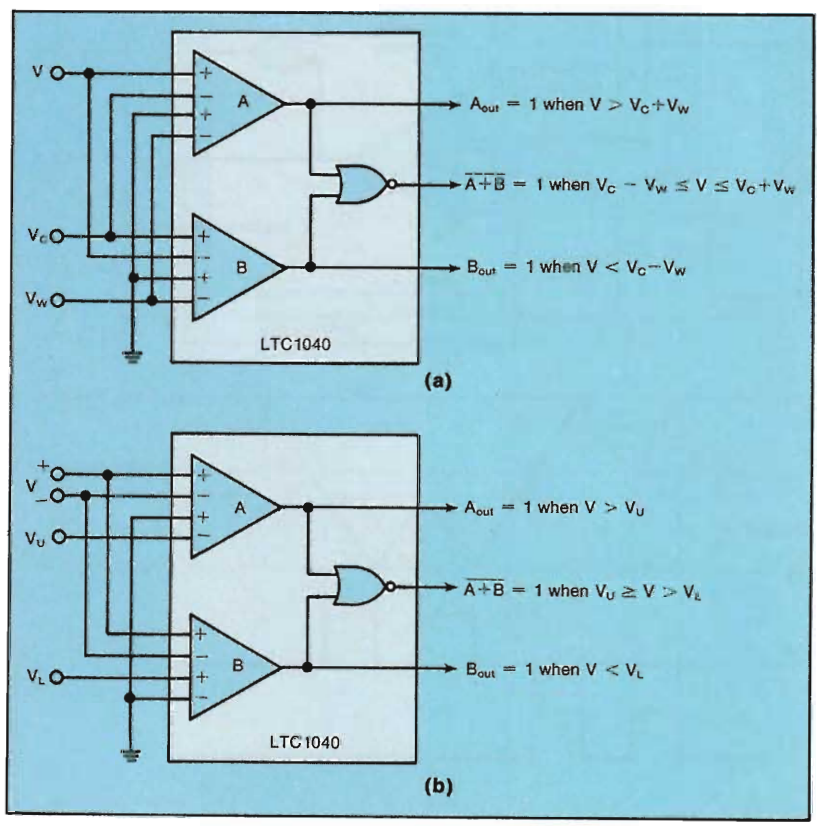
enced to ground.

Conventionally, comparing, say, a bridge's voltage to a trip point requires three op amps—two to convert the bridge output into a single-ended signal and a third to compare the bridge voltage with a ground-referenced trip voltage (Fig. 2a). The new comparator, however, achieves the same end by merely tying the bridge directly to one of its differential inputs and the trip voltage to the other (Fig. 2b).

Additionally, the chip's switched-capacitor inputs eliminate a problem common to comparators. With any traditional differential amplifier a permanent offset shift occurs when large differential input voltages are applied for an extended period of time. That shift is not a problem for op amps, because negative feedback forces their inputs to the same potential. But comparators lack such feedback and commonly display large differential input voltages. The dual comparator's switched input stage, though, corrects for any changes in offset that usually occur with time, temperature, and common-mode voltage.

All in all, the chip's features make for unusual ease and flexibility when putting it to work in divergent settings, including window and hysteresis comparison circuits. The purpose of one configuration, which calls for no additional parts, is to indicate the relation of an input voltage, V, to a voltage span, or window. Voltage V_C sets the center of the window, and its width is twice the window voltage, V_W (Fig. 3a). When V is above the window, comparator output A is high; when V is within the window, $\overline{A+B}$ is high; and when V is below the window, B is high. Moreover, the window's width stays the same, regardless of where the center is set.

The input voltage also can be detected differentially. Separate ground-referenced voltages, V_U and V_L dictate the upper and lower limits of the window (Fig. 3b). This arrangement is especially useful for a



3. Sensing voltages above, within, and below a voltage span, or window, is a simple matter for the dual-comparator chip. The input voltage, V, is referenced to ground, and the window's center and width are specified by two voltages, V_C and V_W (a). For greater flexibility, the sensed input can be a differential voltage, and the window's upper and lower values, V_U and V_L, can be separate voltages (b).

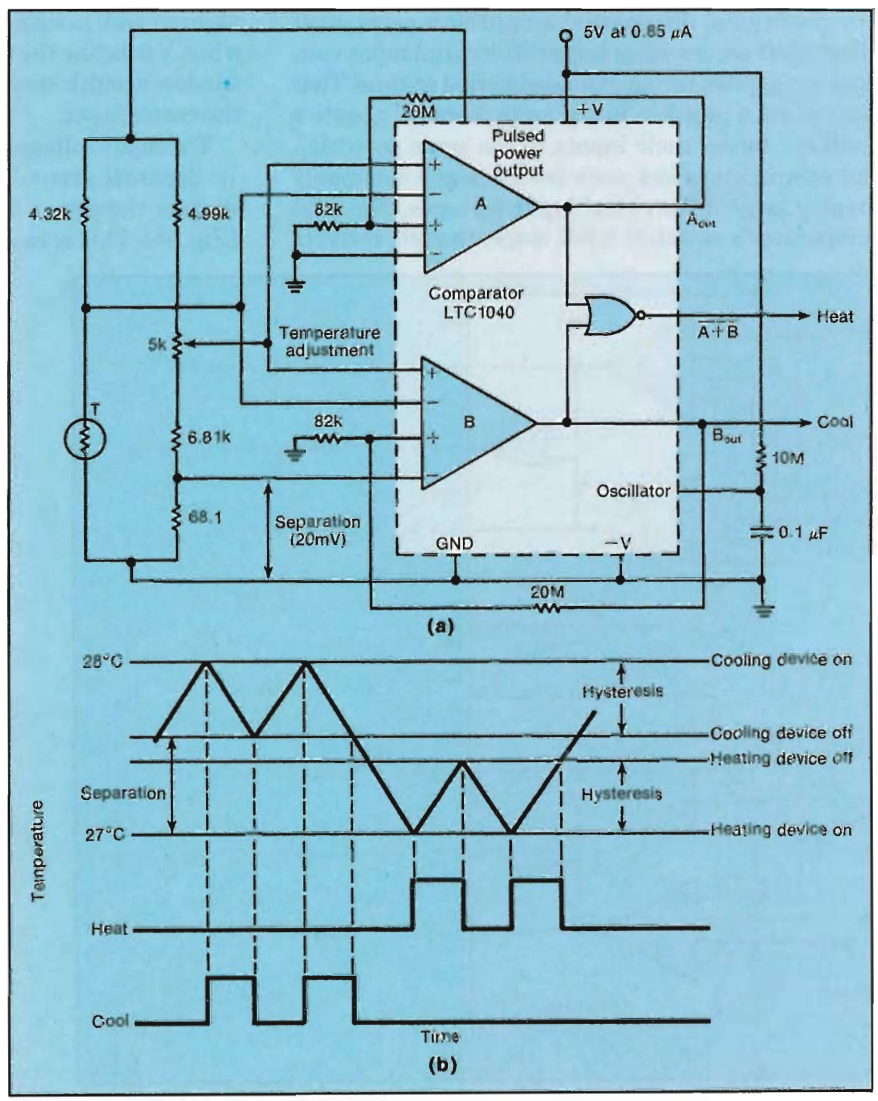
Dual comparator chip

bridge network's differential output or when the accuracy of a ground-referenced voltage suffers from IR drops.

When high gain is involved, adding hysteresis to a comparator circuit frequently prevents spurious, noise-induced switching. A small amount of positive feedback is an effective way to create such hysteresis, but—for conventional comparators—it also presents two problems. For one, the required resistor network on the noninverting input tends to load the voltage source and introduce errors. A 1-MΩ load, say, driven by a 10-kΩ source would yield a 1% error.

Equally bad, the amount of hysteresis changes with a comparator's output swing. Most comparators have open-collector outputs with pull-up resistors and are subject to variations, over time, in gain and saturation voltage, $V_{CE(sat)}$.

To overcome these difficulties, one of the comparator's differential input pairs can be used to set the hysteresis and the other to sense the input volt-



4. A hysteresis comparator is well suited to an automatic thermostat controller. It uses only 5 μW and runs for years on battery power. The desired temperature is set by a 5-kΩ potentiometer and maintained by the controller, which activates heating and cooling devices (a). Hysteresis in the heating and cooling cycles prevents dithering at the trip point (b).

Dual comparator chip

age. The approach eliminates input loading completely because the lightly loaded CMOS output is always pulled between the supply rails. The output goes high at the trip level and low at a set value above that level. As long as the supply voltage is constant, the hysteresis remains fixed. Even if the supply varies, the comparator draws so little current that it can be powered by a separate and independent precision voltage reference.

A hysteresis comparator is of practical value in a thermostat controller. The unit draws only 5 μW and runs for years on battery power (Fig. 4). The desired temperature is set by a 5-kΩ potentiometer and maintained by the controller, which determines whether cooling or heating is required. A thermistor senses the ambient temperature, and a network of 20-MΩ and 82-kΩ resistors establishes the hysteresis for each comparator.

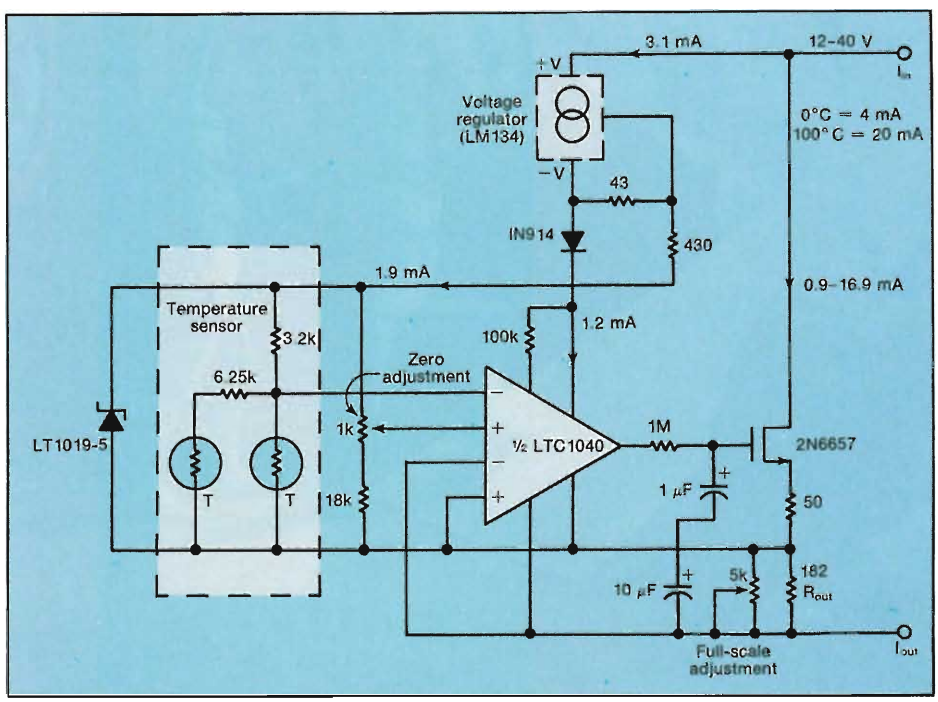
Separate hysteresis loops for the heating and cooling cycles prevent dithering at the trip point. They are set independently both of each other and of a dead band between them. Further, two interlocking mechanisms prevent the system from heating and cooling simultaneously: The hysteresis loops do not overlap, and the NORed output, instead of a direct output, activates the heater. Thus it cannot be turned on during a cooling cycle.

The comparator also serves nicely in a two-wire temperature transducer that requires no external power (Fig. 5). The transducer is driven by the signal current in a standard 4-to-20-mA instrumentation loop and maintains a $\pm 0.3\%$ accuracy from 0° to 100°C.

Two wires do it all

A thermistor network powers the comparator, which adjusts the measurement current by varying a voltage across an output resistor. Specifically, the measurement current is adjusted by altering the gate voltage of a FET. The comparator thus operates as a pulse-width modulator whose output voltage is filtered into dc to control the FET. At the same time, a current source protects the comparator from the 40-V current loop by holding the transducer current to 3.1 mA.

Very little current—measurable in nano-amperes—flows from the negative supply voltage. As a result, the comparator chip's negative supply pin can be tied



5. The comparator can be incorporated into a two-wire temperature transducer that requires no external power source. Instead, power is derived from the signal current in a standard 4-to-20-mA instrumentation loop. The transducer's range of 0° to 100°C is accurate to within $\pm 0.3\%$.

Dual comparator chip

to ground, dropping the error in the output sensing resistor to zero. And since the comparator's common-mode voltage extends to the negative supply voltage, one of its differential inputs can sense the current through the output resistor.

With the comparator on hand, it is a simple task to design a detector that shuts a system down when its battery drops below a predetermined level. Further, the circuit dedicates the remaining energy to retaining any data stored in volatile memory.

A vicious circle

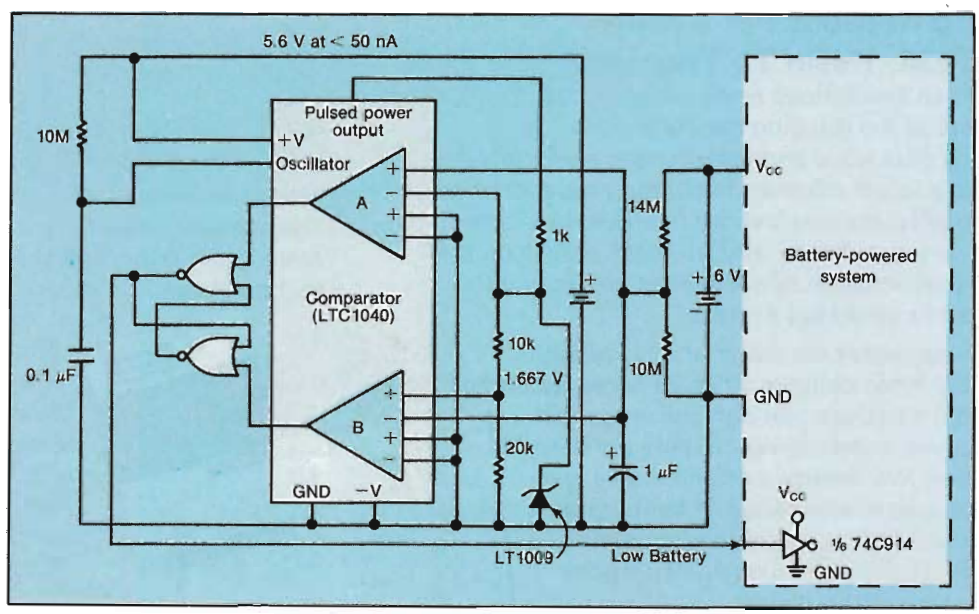
Although any reference and comparator can detect when a battery is low, there are two problems to overcome. One is oscillation. When the battery's load is removed, the voltage goes up, turning the system back on. That causes the battery voltage to drop, and the system to turn itself off again—creating a continuous cycle. Second, a simple reference and comparator circuit might draw too much current for a battery-powered design.

An alternative circuit, powered by two small lithium batteries, plays to the strengths of the dual comparator chip. One comparator is set to a 6-V trip voltage that corresponds to the batteries' fully charged state (Fig. 6).

As they discharge, the comparator's output arms an RS flip-flop. When the battery voltage falls below 4 V, the second comparator sets the flip-flop and the system shuts down. A subsequent increase in voltage does not cause oscillation because the system does not turn on unless completely charged batteries are connected. Only the full voltage will cause the first comparator to reset the flip-flop and reapply power.

Although the correct shut-off and turn-on voltage levels will depend on the type of battery and the load currents drawn for charged and discharged states, these levels can be easily set by resistor ratios. Also, the overall performance depends on the resistors' accuracy, for which 1% is sufficient. No trimming resistors are needed, and the 1% tolerance gives a worst-case resistor error of 2%, more than adequate for a circuit of this type. By comparison, the ±0.02% (±5-mV) tolerance of the zener diode and the ±0.02% (±500-μV) input error of the comparators are relatively unimportant. □

How useful?	Circle
Immediate design application	541
Within the next year	542
Not applicable	543



6. A low-battery detector designed around the comparator chip eliminates the oscillation typically caused when the system is disconnected and the battery voltage rises. Because of built-in hysteresis, before this arrangement will turn back on, fully charged batteries must replace the discharged ones. The circuit itself runs on two lithium batteries, chosen for their long life.

Jim Williams A Mover And Shaker Of All Things Analog

September 13, 2004 12:00 AM
Electronic Design

Doris Kilbane

Today, newborns will often fall asleep to sounds from radios, TVs, CDs, DVDs, etc. But 51 years ago, sleep wasn't in the equation when five-year-old Jim Williams' dad brought home a short-wave radio. It was a "seminal event," as he describes it.

"I can see the Hallicrafters Model S-38 in my mind's eye now. We turned it on and for the life of me, I could not understand how all those voices from all over the world came out of that box," says Williams, designer of hundreds of fundamental analog circuits and prolific author on analog technology.

"I played with it a couple of nights. My dad, not at all a technologist, encouraged me to take the box apart," says Williams. "Mostly I just took it apart and made a mess of it. I never got it together again, yet that episode transfixed me. I did not wonder what I would do with the rest of my life. There was no question."

Williams became transfixed over electronic circuits, to the detriment of his schoolwork. "Instead of doing my homework, I read the HP catalog about their test equipment and electronic instrumentation," he says. At 13, he even applied for a job at HP, but it turned him down. "I spent my youth building and debugging circuits at home and working in TV shops," says Williams. The author of more than 250 articles on analog circuit design didn't know they were analog circuits. "To me they were just circuits," he says.

From 1958 to 1979, Williams set up shop at the Massachusetts Institute of Technology. There he concentrated exclusively on analog-circuit design, specifically the application of analog-circuit techniques to biochemical and biomedical problems. Work included ultra-stable temperature control for biochemical microcalorimetry, a precision scale for human metabolic studies, feedback control of fermentation processes, and instrumentation development for cell separation and counting.

At the same time, he acted as a consultant for U.S. and foreign governments and corporations about analog circuits. Assignments included analog-circuit development, design review and assistance, and application literature generation.

Williams joined National Semiconductor Corp. in 1979 and continued his assault on analog circuits as part of the Linear Integrated Circuits Group. During this period, he set about marrying analog and digital technologies, publishing a processor-corrected one-part-per-million accurate analog-to-digital converter.

Staff scientist at Linear Technology Corp. since 1982, Williams has concentrated on product definition, development, and support. He's responsible for in-house and customer support across Linear Technology's entire product range. Looking back, Williams sees the change in attitude about the value and necessity of analog circuits as his most significant impact on the engineering field.

"Go back 20 to 25 years, and the conventional wisdom was that analog techniques were fundamentally unnecessary," says Williams. "This was heralded by the advent of microprocessor-based techniques. It was thought that digital technology had rendered analog technology obsolete. Another group of people thought the digital revolution was real and significant, but they didn't believe its advent meant analog technologies were dead. Then and now, I'm a member of that group. I tried to demonstrate that analog technology would serve as a useful adjunct to digital techniques."

Then, Williams rather laughs at himself and adds, "Luckily for me, too, because I didn't have a choice. Analog technology is what I did and like to do, but I also had to sell it." And sell it he did. He wrote article after article, taking every advantage to demonstrate its value to the trade press. He explained how "very useful it was to support hardware," and he editorialized at every opportunity. Williams says that "there were a fair number of opportunities present to editorialize about the issue, and I made sure to take advantage of them."

What was the result of that? "It kept me employed," he laughs. Then he gets serious. "People took a second look and found there were things needed in systems and circuit boards that were fundamentally analog in nature."

Now, do people understand the need and value of both technologies? Yes, digital still gets the glitz and glamour in the headlines. But people now acknowledge that analog plays a needed supportive and enabling role. "No one is declaring analog technology dead anymore," he says.

More analog circuits are built today than at any other time. The digital revolution did analog a favor, notes Williams. Every digital box contains analog circuitry.

After a lifetime in the analog field, are there still challenges? Most definitely, according to Williams. "My goals are still pretty much the same. Find technical things to do that I think are interesting, that customers need and that Linear Technology wants done, and try to do it for them."

He's now working on problems relating to getting high-quality photographic capability into cell phones with particular lighting. "We're making xenon lighting usable in cell phones. Xenon 'flash' illumination is hundreds of times brighter than other light sources. The challenge is the space and cost issues with these high-powered circuits. You can get it to work, but the question is how to do it in a phone at an attractive price," says Williams.

Williams strives to bring improvements to the world outside the realm of analog circuits, too. "I support charitable groups through private, targeted donations. If I see something I don't like and can try to change it by supporting a group or cause, I go ahead and do it." He also supports various medical organizations and education at specific universities.